Wafer-level CMOS post-processing

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Integrated circuit technology bears the promise to fabricate minute, smart sensor systems in large quantities for an attractive piece price. In this presentation, recent developments will be discussed that enable integrated pixel sensors in CMOS microchips. The fragile nature of a CMOS chip sets the boundary conditions for post-processing, whether on a wafer or on a single chip. Only a small subset of planar technology manufacturing steps qualify to be used in this stage. With the introduction of chemical mechanical polishing, SU-8 photoresist technology, atomic layer deposition, and ECR-CVD and ICP-CVD, new possibilities arise to fabricate sensing elements on top of an integrated circuit. Several options for photon and particle detection will be addressed, based on the present possibilities in CMOS-compatible post-processing.