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Design and test of an integrated Sigma-Delta analog-to-digital converter for X-ray Computed Tomography

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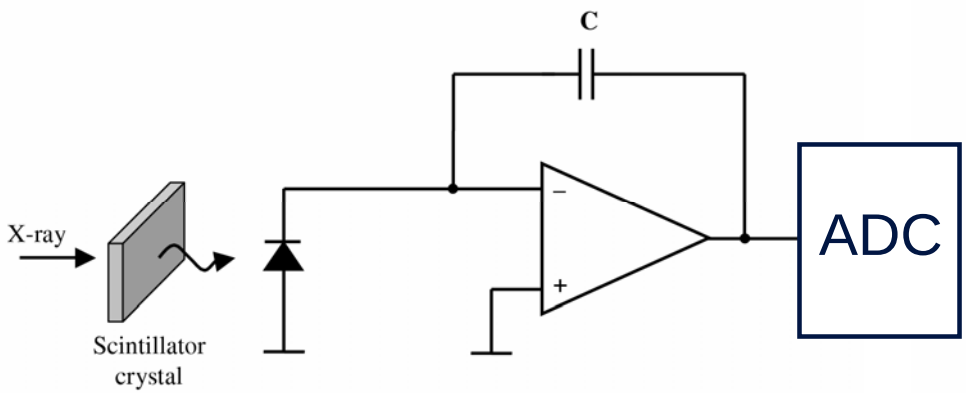
Outline

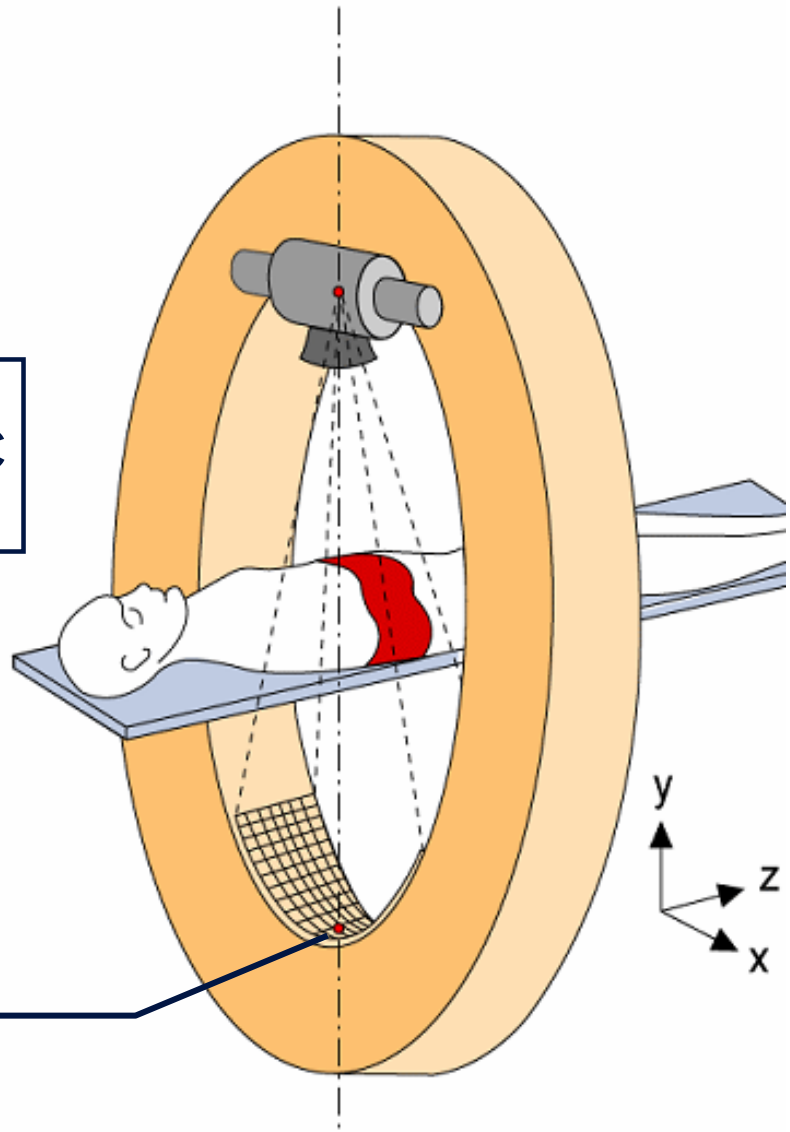
- Introduction to Computed Tomography
- Realization of a ‘digital pixel’
- Experimental Results
- Design of a Decimation and Low-pass Filter for CT
- Conclusion and Outlook

CT Principle

Detector channel (generically):



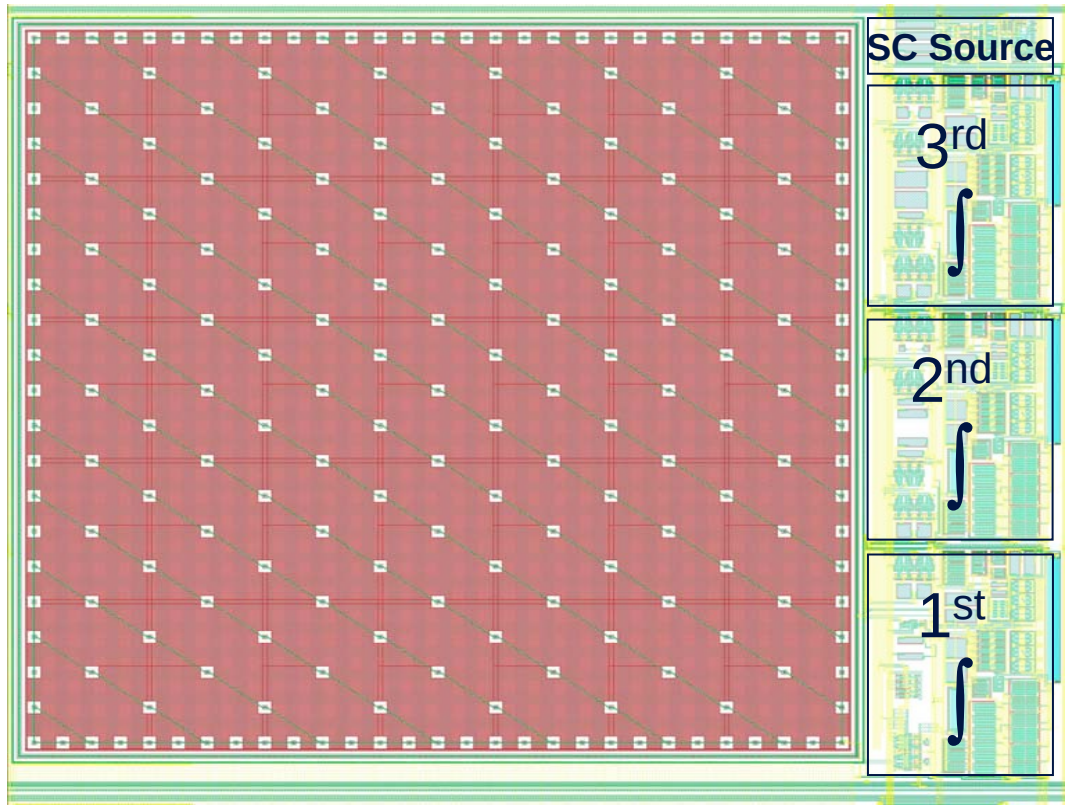
- indirect conversion
- sample and digitize photocurrent (13 pA to 174 nA)



Overview: in-pixel ΣΔ modulator

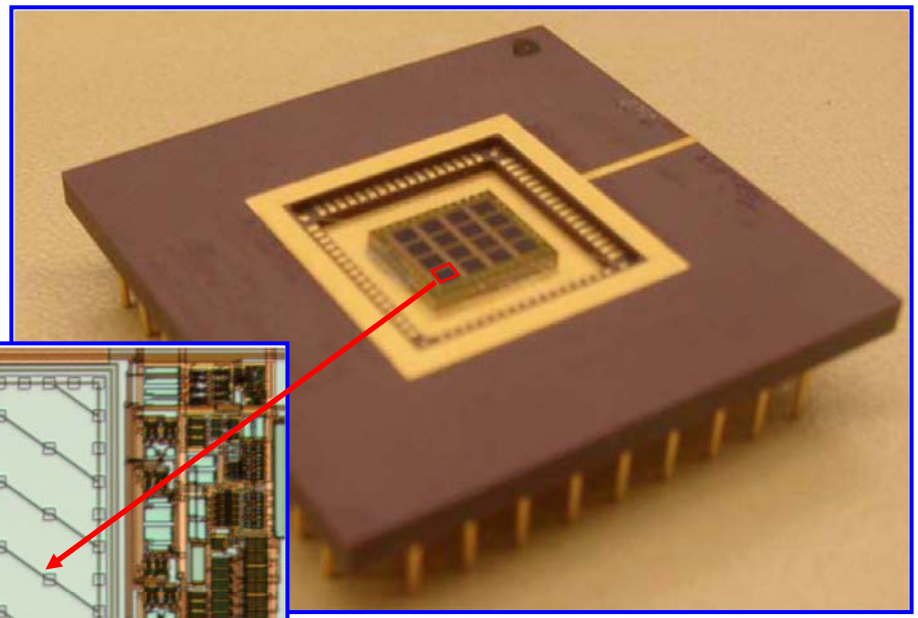
- **Specifications:**
  - photodiode and electronics combined in digital pixel (monolithic approach)
  - 10 kHz bandwidth
  - 4x4 pixel array

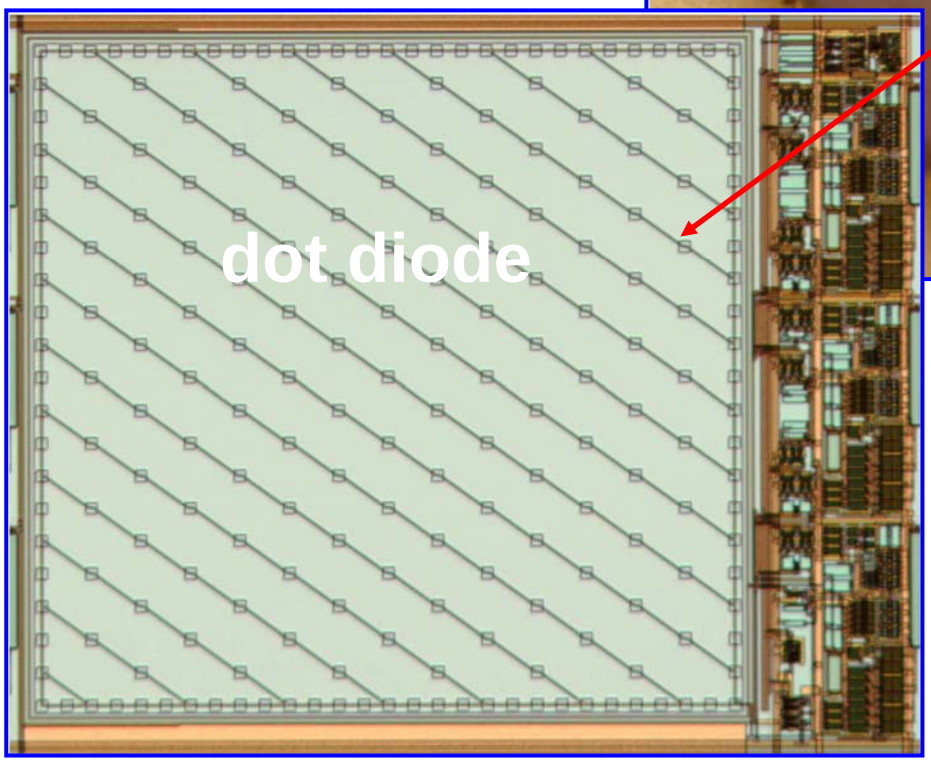
- **Design Issues:**
  - 3rd order modulator
  - f_s = 3 MHz (oversampling ratio OSR =150)



Test structures of in-pixel ΣΔ modulator

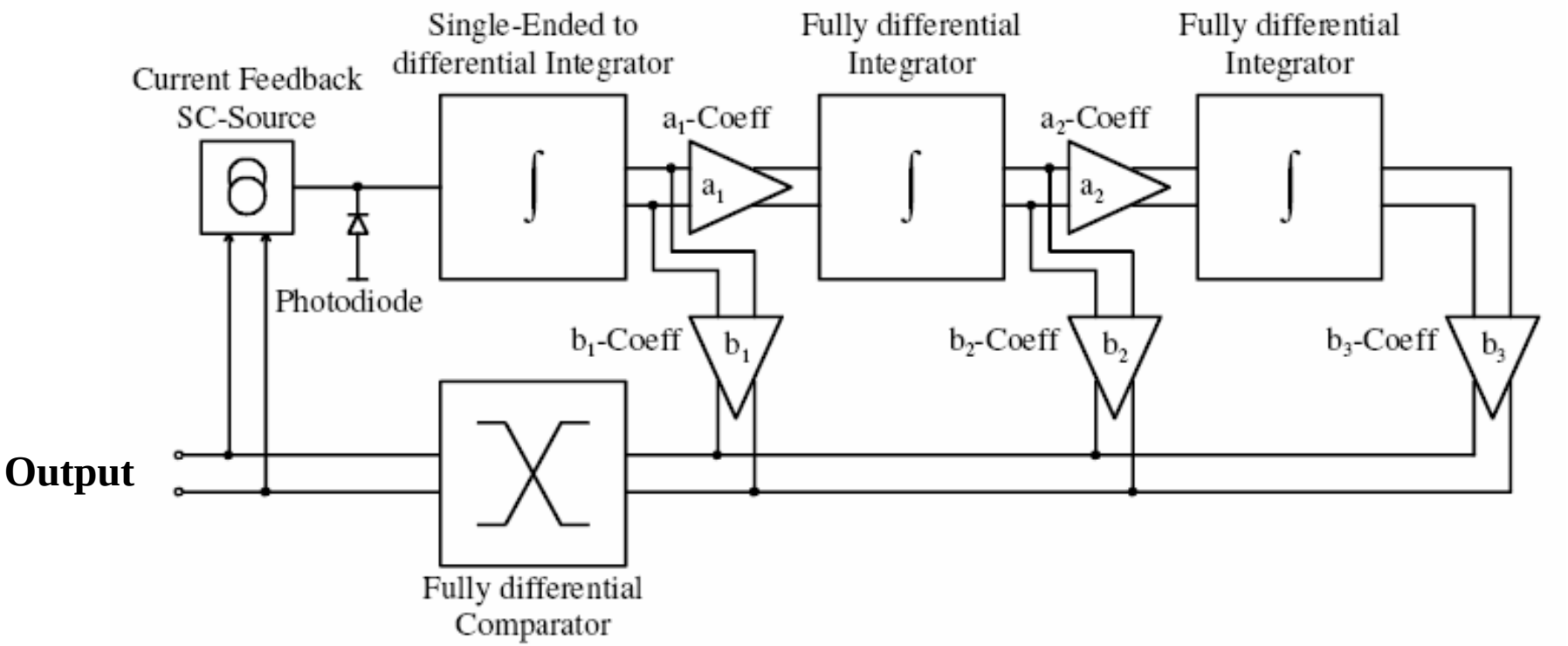
low capacitance photodiode (≈ 7 pF)





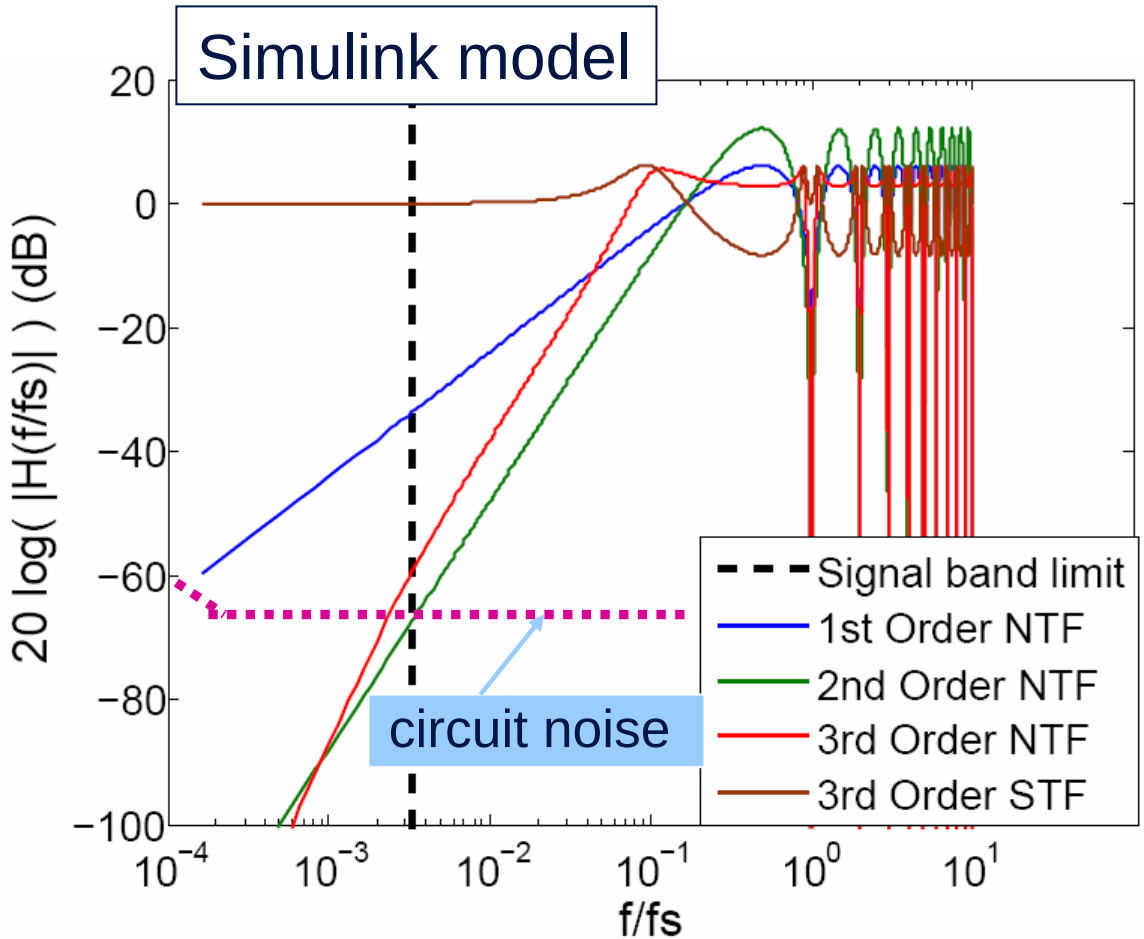
first test samples in PGA package with open lid

ΣΔ-modulator: Implementation



- feedforward structure of feedback loop, 1-bit quantizer
- driven by 2 non-overlapping clocks (3 MHz)
- differential design
- switched-capacitor implementation, 0.8 μm CMOS process

Quantization noise of ΣΔ-modulator

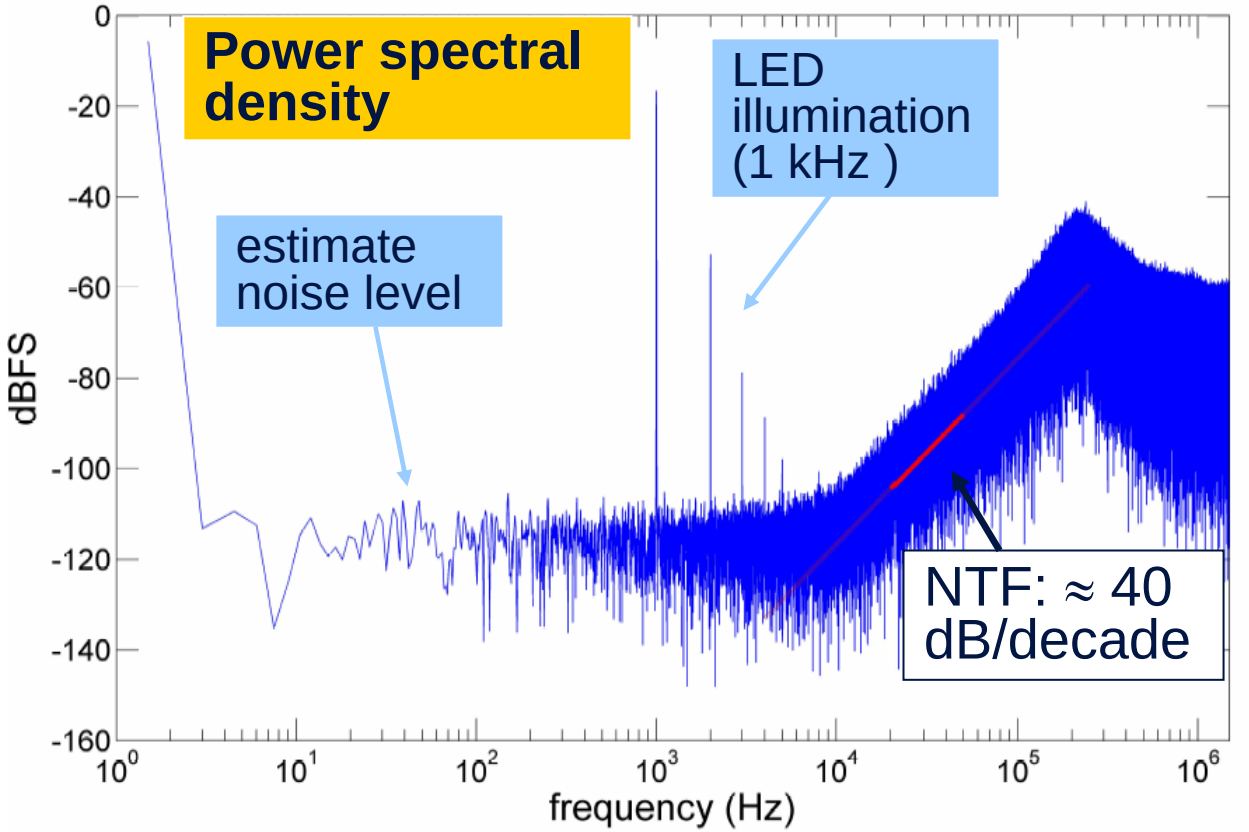


NTF = noise transfer function
STF = signal transfer function

Result:
Implemented modulator is 3rd order in signal-band and 2nd order above

Noise shaping: shift quantization noise to higher frequencies (modulation noise)

Experimental results: Power Spectra



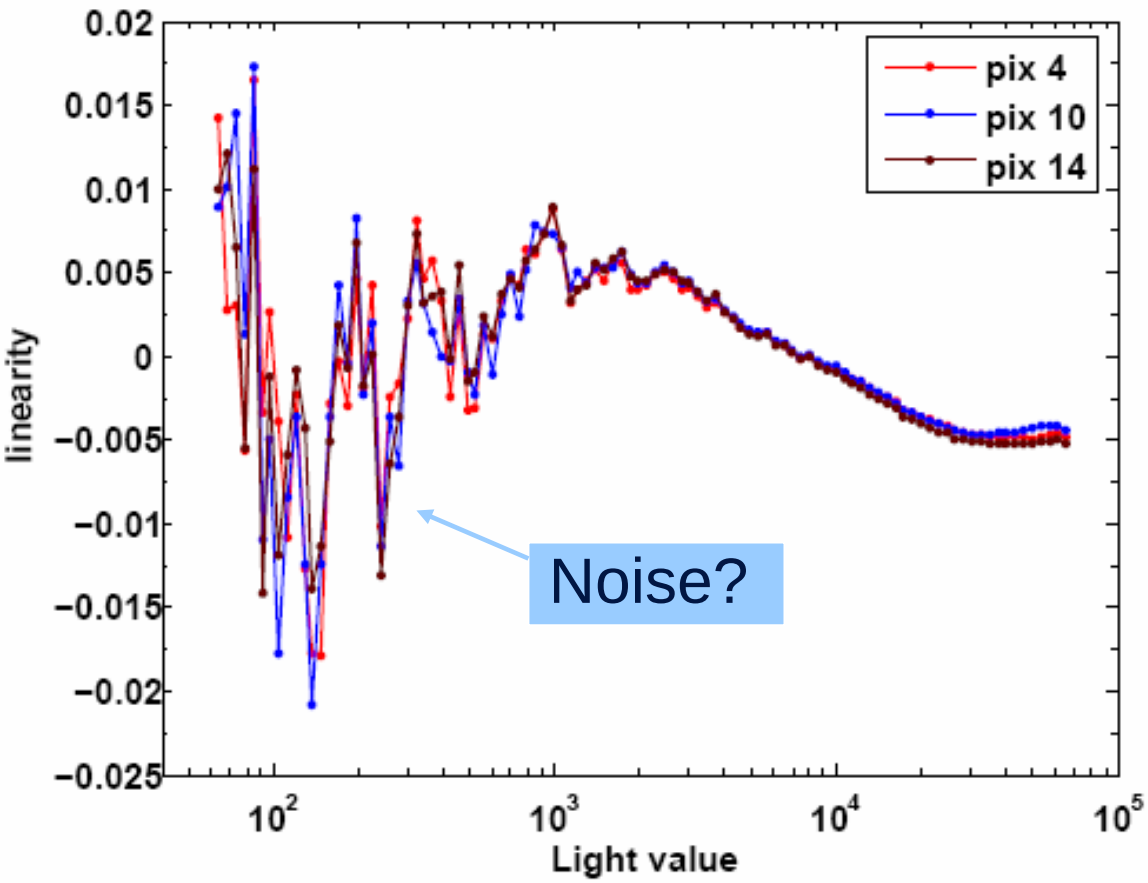
track down excess noise to circuit design!!!

➔ Spectre (Cadence) full analog extracted simulation reproduces electronics noise!

Results:

- bandwidth ≈ 10 kHz
- gradient of NTF according to theory
- noise level ≈ 20 pA_{RMS} @10 kHz, factor > 3 higher than predicted!

Experimental results: Linearity of digital pixel



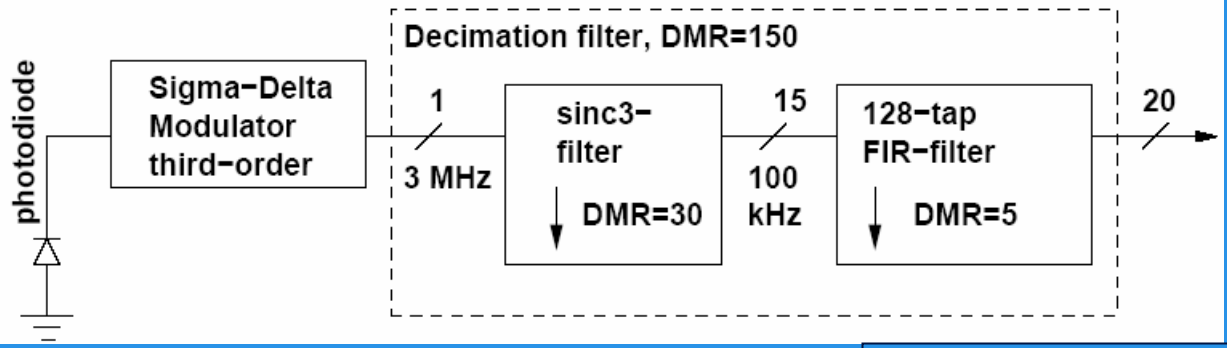
Measurement:

- Linear light source (DC)
- infrared filter and integrating sphere
- reference photodiode and Keithley pA-meter
- measurement protocol of descending light values

<u>Conclusion:</u> still limited by experimental setup!

Decimation Filter Design

2-stage filter structure sinc^3 + FIR filter:

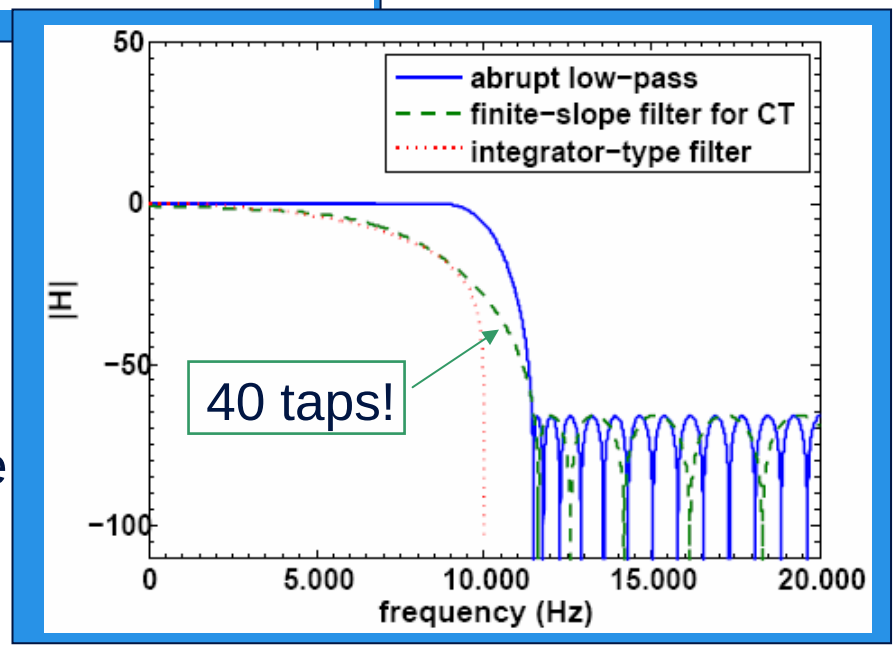


Tasks:

- attenuate noise
- linear phase filter (signal)

hardware costs:

- 1st stage: sinc^3 filter sufficient
- 2nd stage:
  - ≈ 100 tap-FIR filter for boxcar-type filter
  - 30-40 tap -FIR filter for sinc-type filter up to first zero

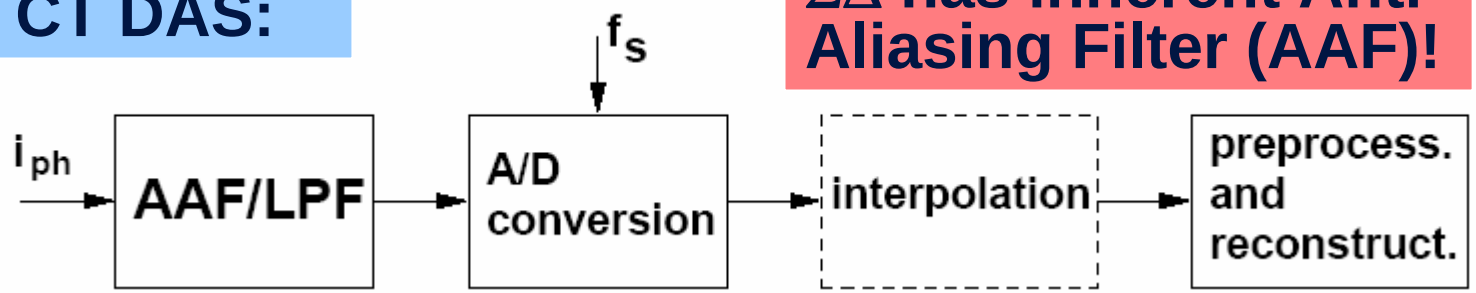


Frequency Response: ΣΔ vs. Integrator

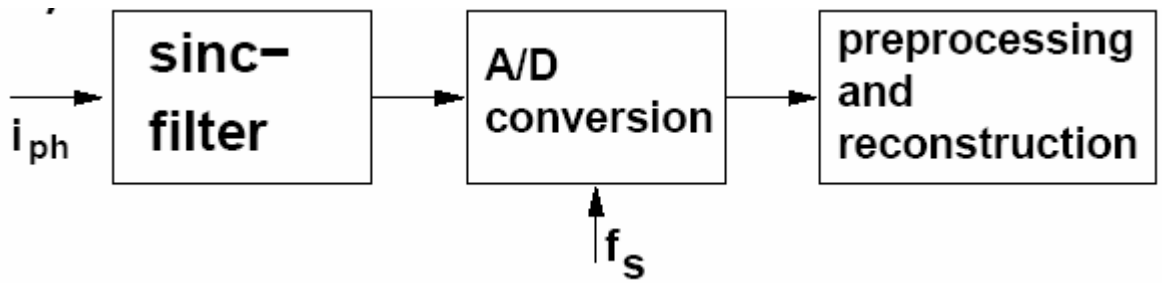
Filter operation has effect on noise and **signal !**
Top-level view of ΣΔ ADC and Integrator-type ADC:

ΣΔ operation in CT DAS:

ΣΔ has inherent Anti-Aliasing Filter (AAF)!



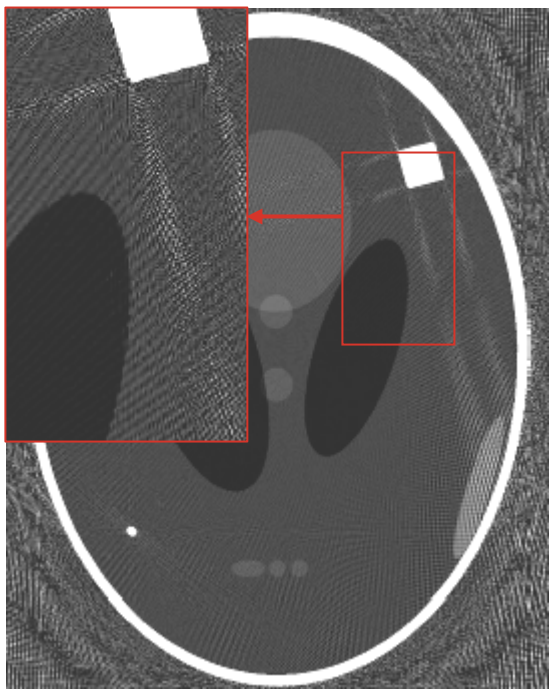
Integrator + ADC in CT DAS, e.g. current-to-frequency converter, DDC11x:



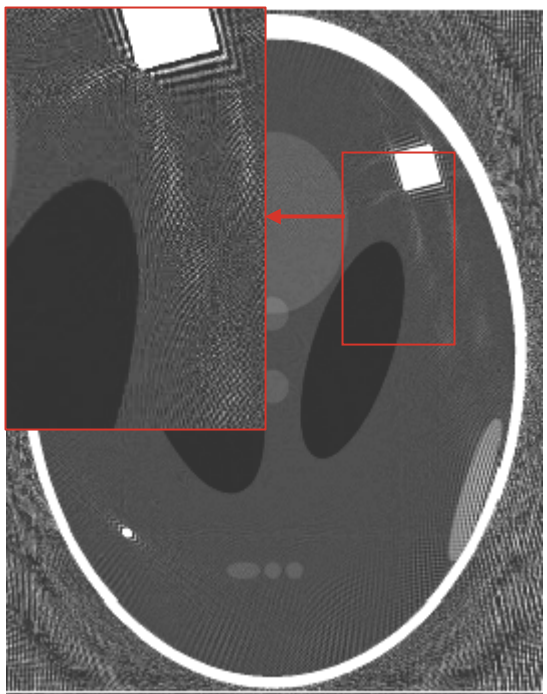
Impact of Filter Operation on Reconstructed Images

- simple simulation with 500 views per rotation (FBP)
- Apply different filter structures to detector signals in time domain!

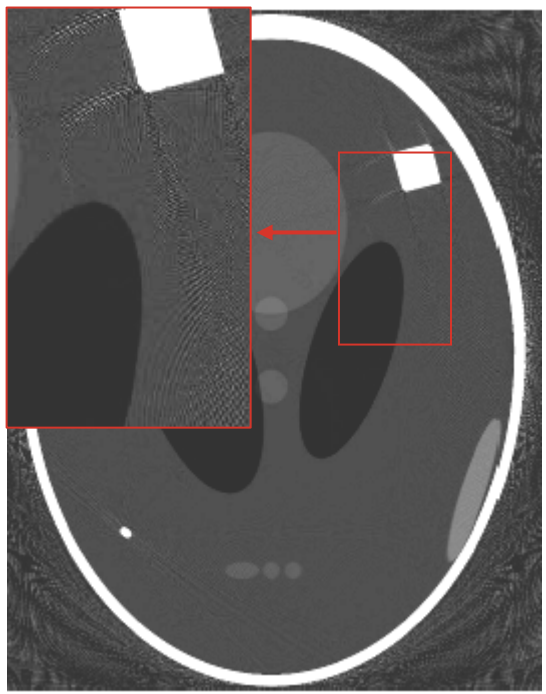
Integrator



ΣΔ, boxcar-filter



ΣΔ, sinc, full bw



Summary and Outlook

- Samples of ΣΔ-based CMOS digital pixel operational and succesfully been tested
- Bandwidth, linearity (< 1%) according to specs, SNR too low!
- Excess noise attributed to circuit non-idealities (simulations, counter-measures proposed)
- Decimation filter designed and implemented in FPGA

- ΣΔ-converters provide means to tailor frequency response in rotational direction!
- Outlook: low-power design
- Outlook: more logic into pixel, e.g. with 0.35 μm CMOS process with high voltage option

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