Development of 3D detectors and SiPM @ ITC-irst

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ITC-irst

ITC (Istituto Trentino di Cultura) is a public research institute in Trento mainly funded by the local government

ITC-irst

250 researchers working on:

- information technology
- microsystems & physics

An entire division (60) is working on silicon sensors

Silicon Radiation Detectors R&D activity

TCAD simulation
CAD design ⇨ Fabrication ⇨ Device testing

“Standard” technology

From the specifications given by the “user”
we design, produce, and (electrical) test the detector.

- **single/double-sided strip detectors**
- **p-on-n/n-on-n pixel detector**

R&D activities

Development in cooperation with the partners

- **very thin detectors**
- **detectors made on radiation hard silicon substrates**
- **3D detectors**
- **silicon photomultipliers**

▶ Development of 3D sensors and SiPM is being carried out in the framework of a collaboration between INFN and ITC-irst

MT - LAB

Furnaces

We process 4” wafers

MICROFAB. LAB.

- Ion Implanter
- Furnaces
- Litho (Mask Aligner)
- Dry&Wet Etching
- Sputtering & Evaporator
- On line inspection
- Dicing and bonding

Automatic probe station

(cassette-to-cassette double side testing)

TEST LAB.

- Automatic probe station
- Manual probe station
- Optical bench

Development of 3D detectors @ ITC-irst

3D - Outline

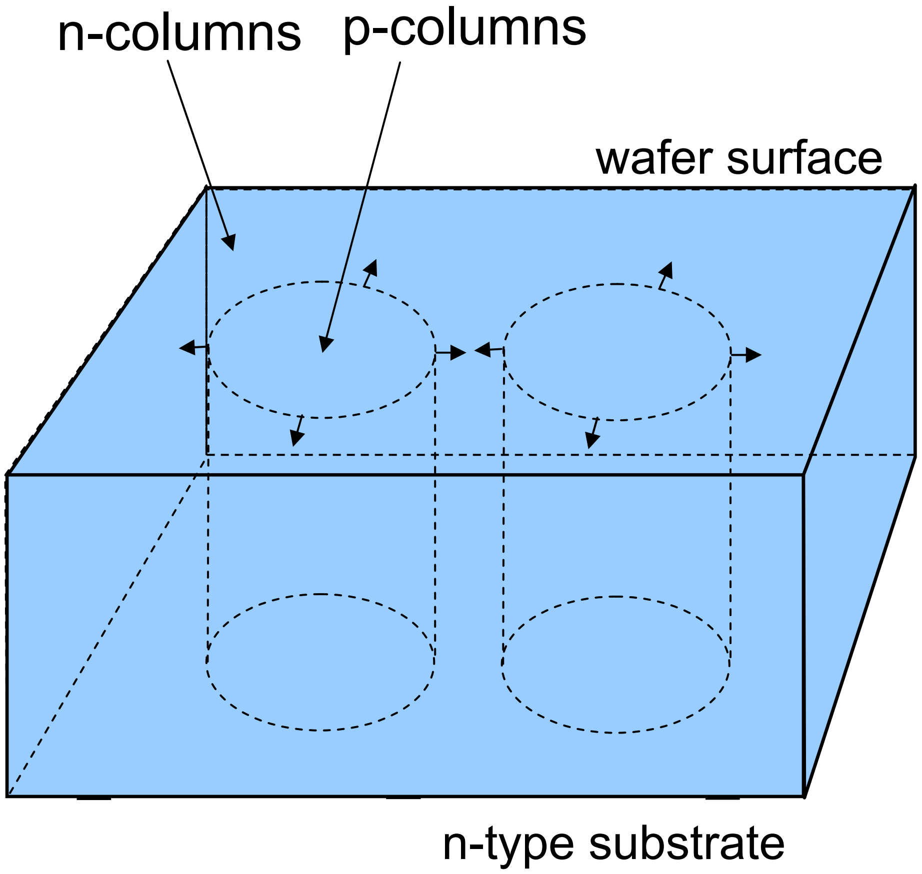
- “standard” 3D - concept
- 3D detectors: status

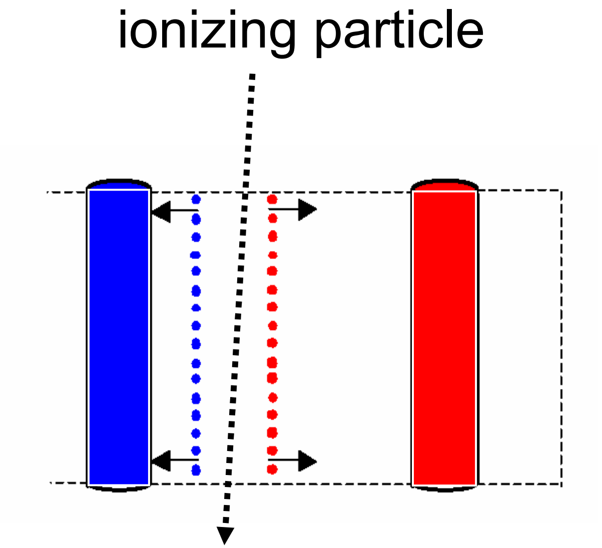
ITC-irst activity

- Single-Type Column 3D detector concept
- Simulation, Design, Process and First Characterization
- Future Activity

“Standard” 3D detectors - concept

Proposed by Parker et al. NIMA395 (1997)





Short distance between electrodes:
- low full depletion voltage
- short collection distance

➡ more radiation tolerant than planar detectors!!

3D status

- SLAC (*Sherwood Parker*)

double columns filled with doped polisilicon, deep hole (entire wafer thickness)

- University of Glasgow

double columns Schottky & diffused diode, deep hole ,
more info on http://rd50.web.cern.ch/rd50/5th-workshop/

- VTT

Semi 3D: single column boron doped on n-type Si; limited depth (150-200μm)

- ITC-irst

Single Type Columns: single column phosphorus doped on p-type Si; limited depth (150-200μm).

- CNM

workshop on 3D in february 2006 at Trento : http://tredi.itc.it/

3D detectors @ ITC-irst

1. Simulations of 3D-STC detectors

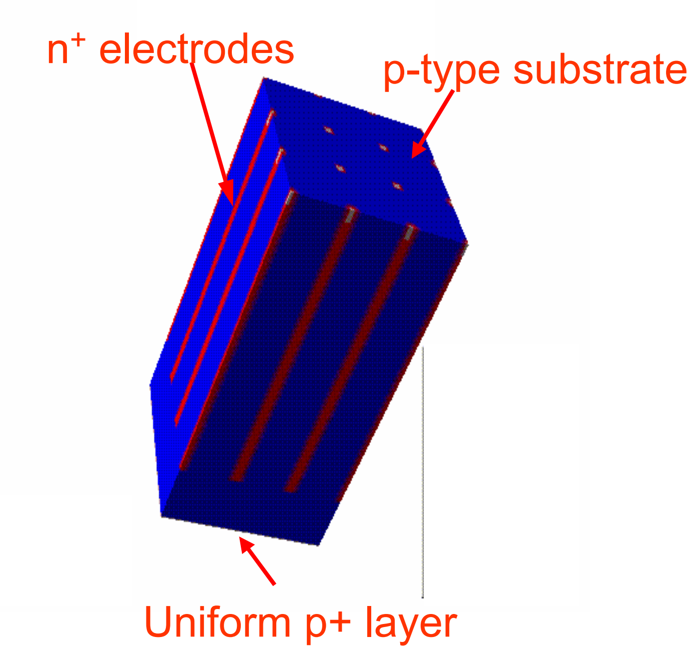
2. Technology used in the first two fab. runs

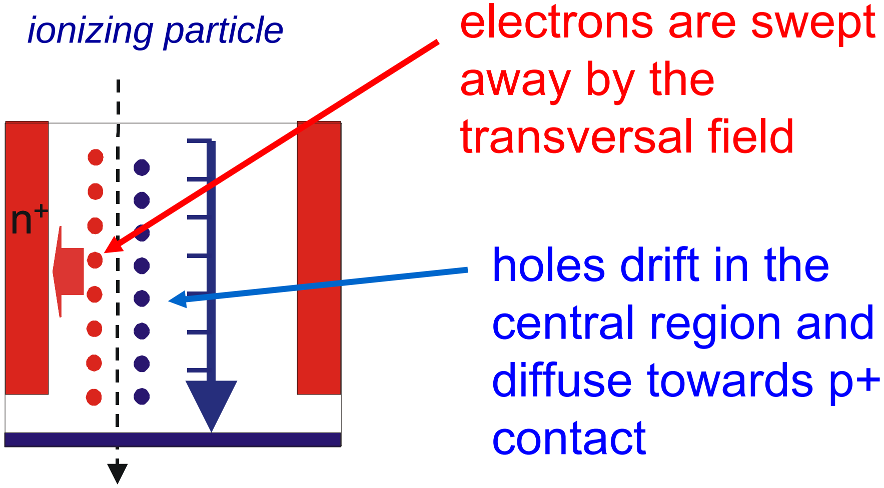
3. Electrical characterization of first prototypes

4. Future Activity on 3D

Single-Type-Column 3D detectors - concept

NIM A 541 (2005) 441–448 “Development of 3D detectors ..” C. Piemonte et al





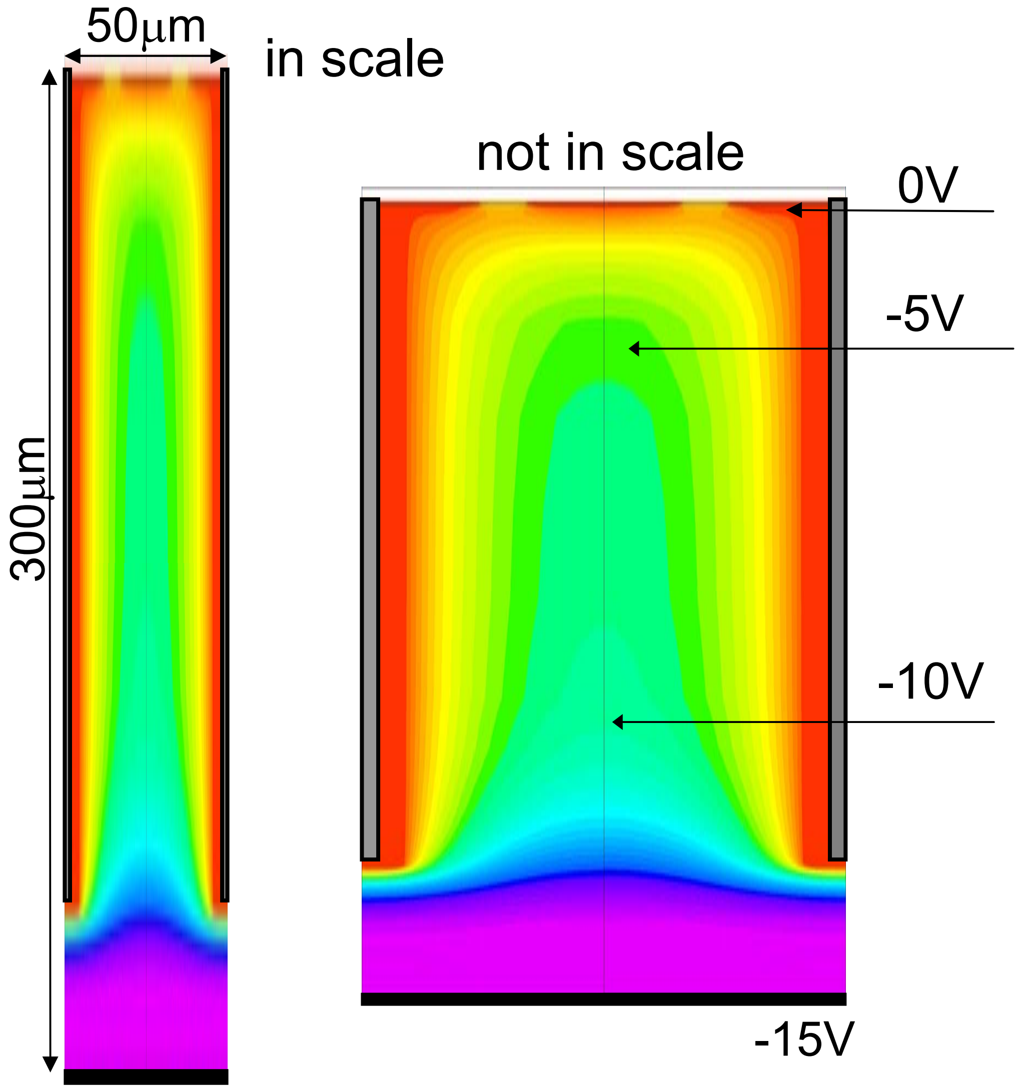
Main feature of proposed 3D-STC:

- column etching and doping performed only once
- holes not etched all through the wafer
- bulk contact is provided by a backside uniform p$^+$ implant

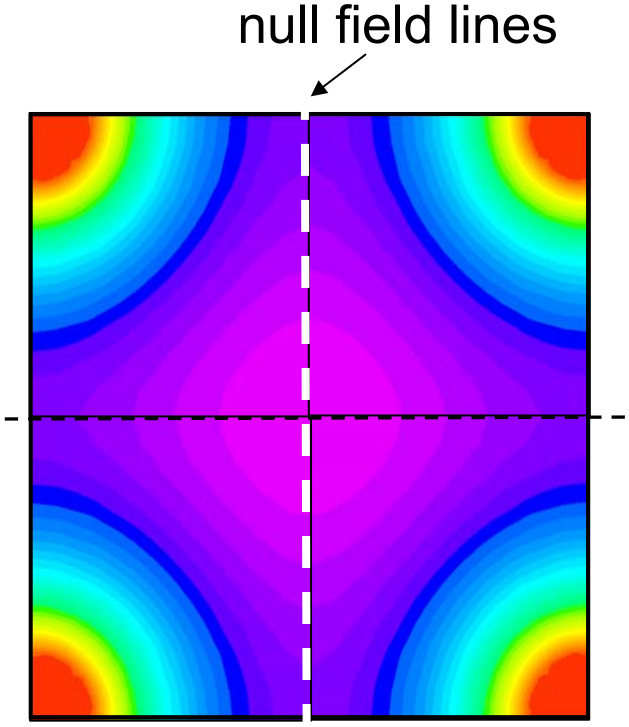
⇒ Simplification of the fabrication process

Simulated potential distribution (1)

Potential distribution (vertical cross-section)

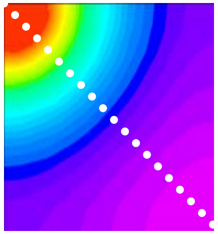


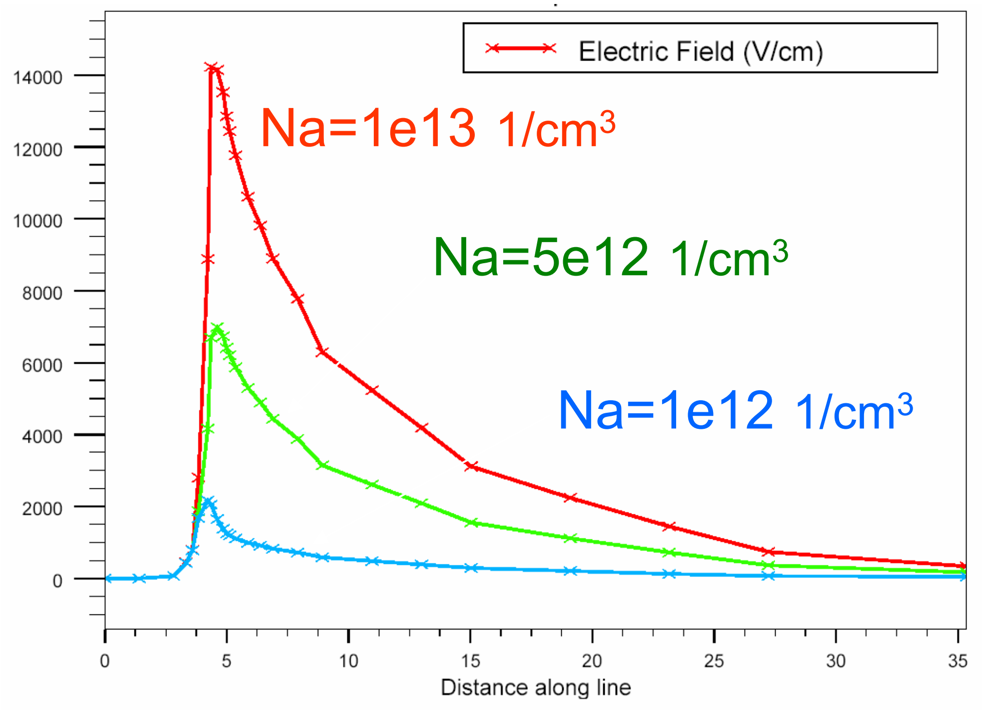
Potential distribution (horizontal cross-section)



Simulated potential distribution (2)

Simulation of the electric field along a cut-line from the electrode to the center of the cell





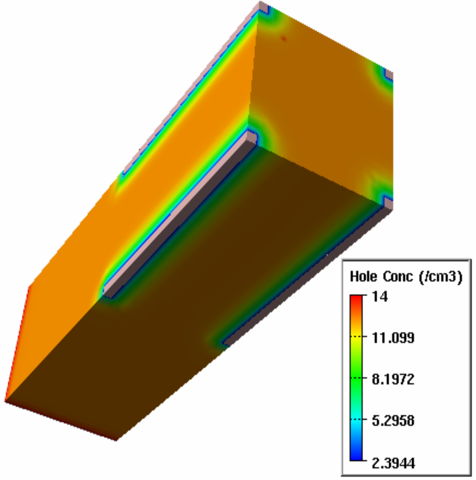
DRAWBACK:

3D-stc: once full depletion is reached it is not possible to increase the electric field between the columns

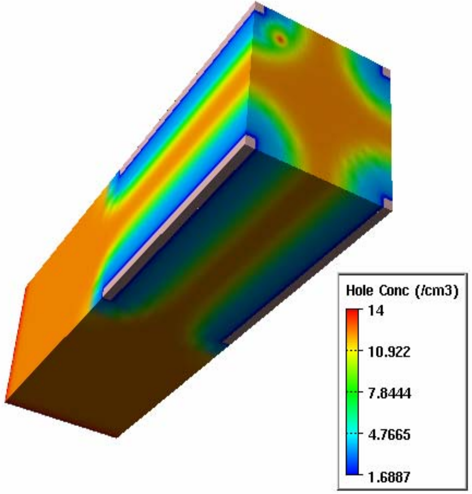
To increase the electric field strength one can act on the substrate doping concentration

Capacitance simulations

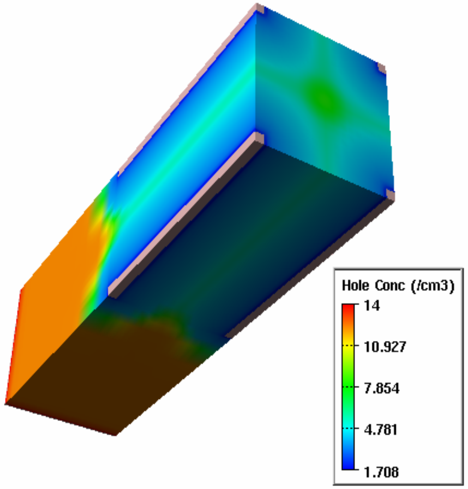
1) V_{bias}=0V



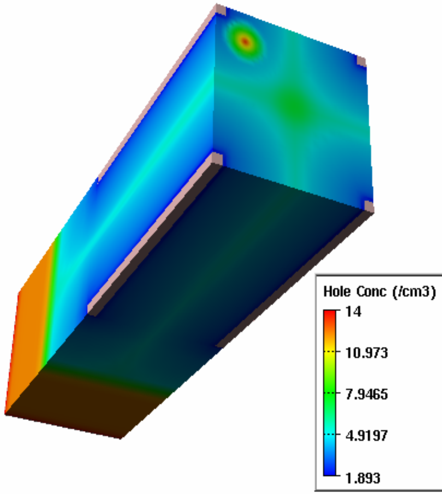
2) V_{bias}=2V



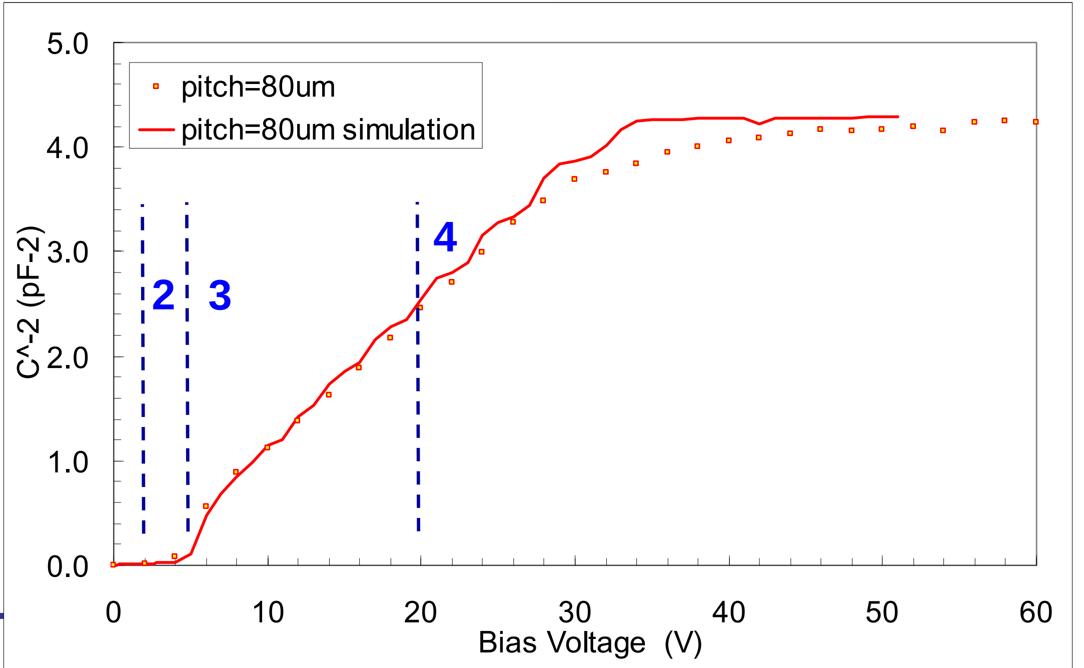
3) V_{bias}=5V



4) V_{bias}=20V



Do not consider the hot spot in the pictures, it is the charge released by a particle.

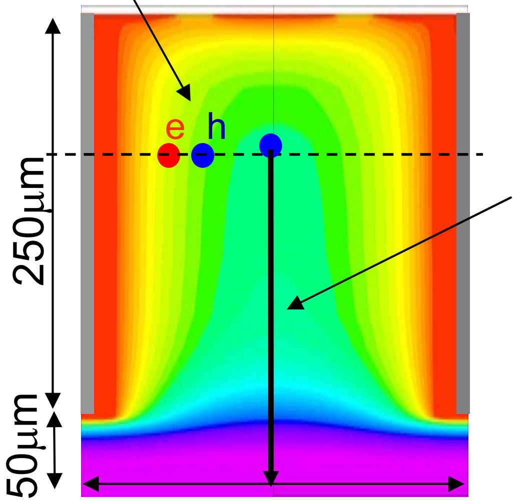


The $1/C^2$ curve of the col-to-back capacitance can be used to extract both the intercolumn as well as the col-to-back full depletion.

Full charge collection time

First phase

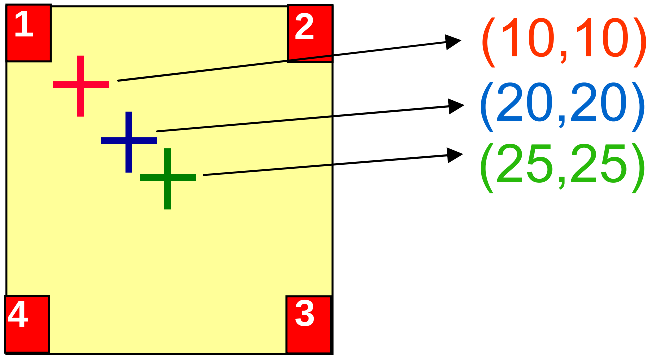
Transversal movement

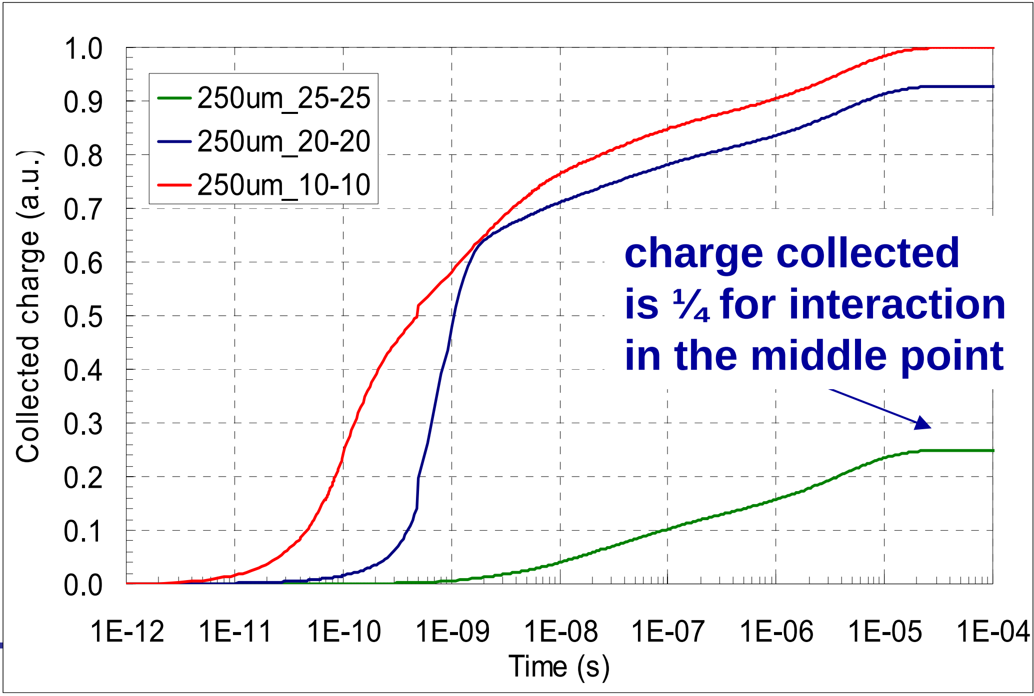


Second phase

Hole vertical movement

Same V_{bias}, different impact point



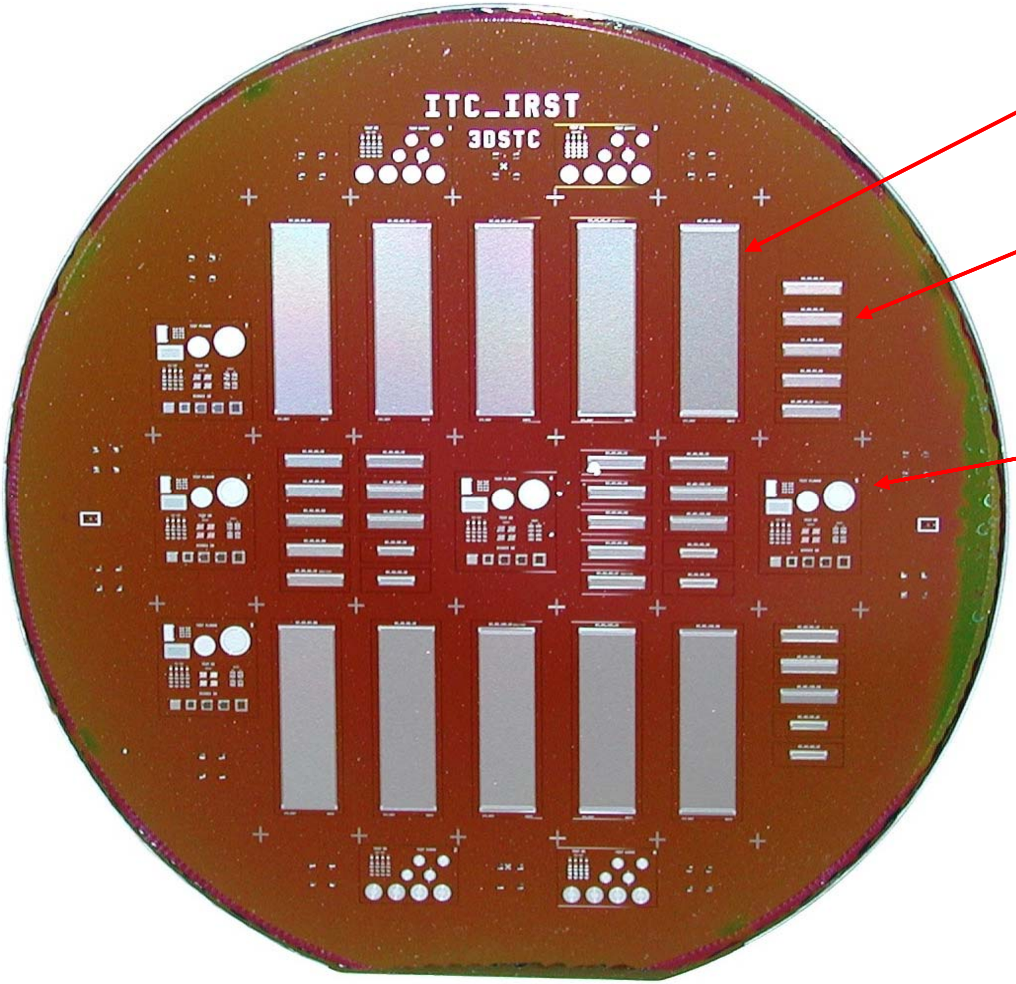


charge collected is ¼ for interaction in the middle point

In the worst case of a track centered the central region, 50% of the charge is collected at t ~ 300ns

Outside this region, 50% of the charge is collected within 1ns.

Mask layout



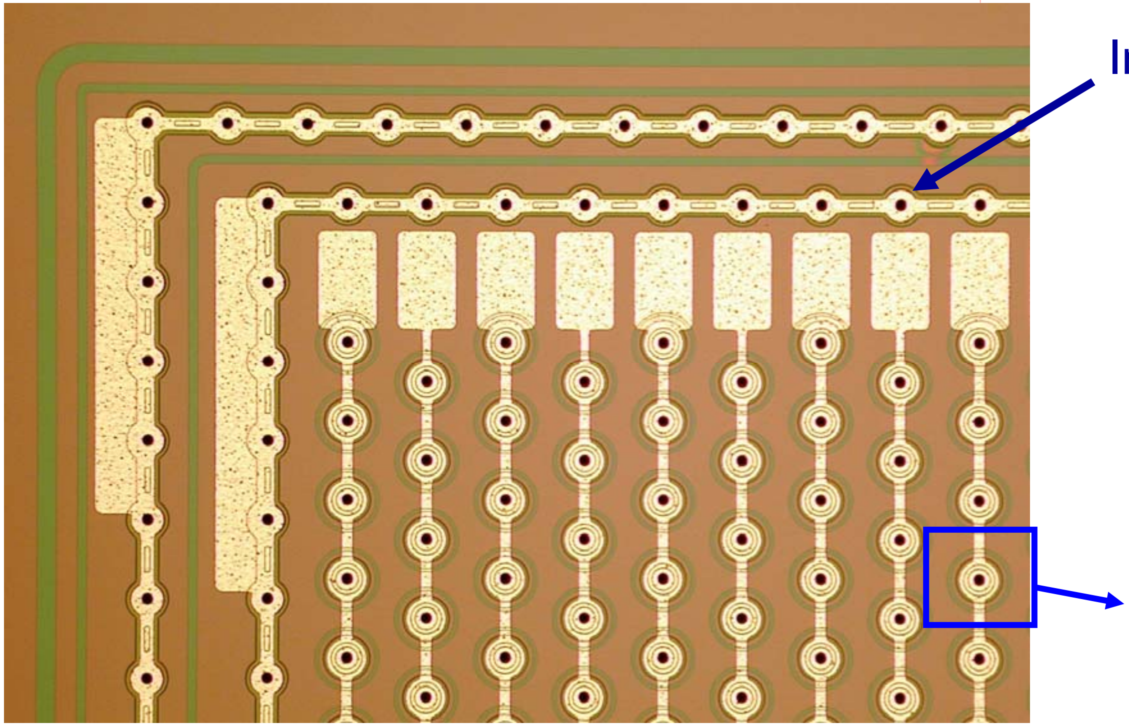
“Large” strip-like detectors

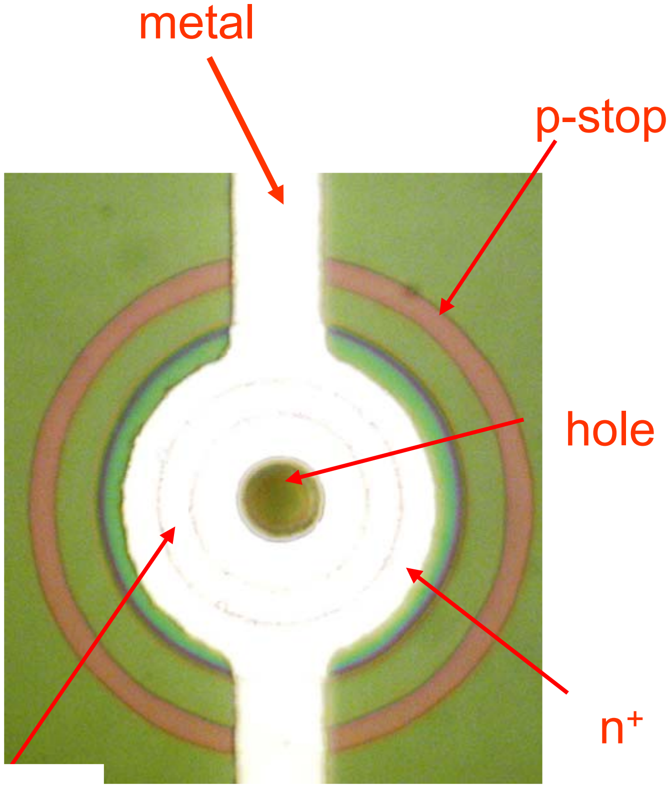
Small version of strip detectors

Planar and 3D test structures

1. “Low density layout” to increase mechanical robustness of the wafer
2. Strip detector = “easy” to electrical test

Strip detectors - layout





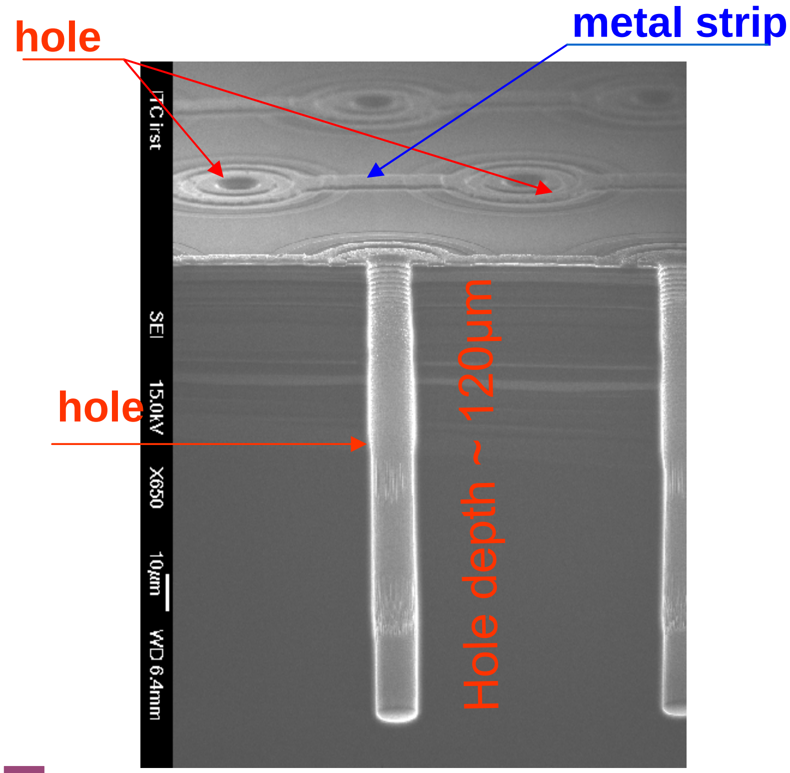
Different strip-detector layouts:

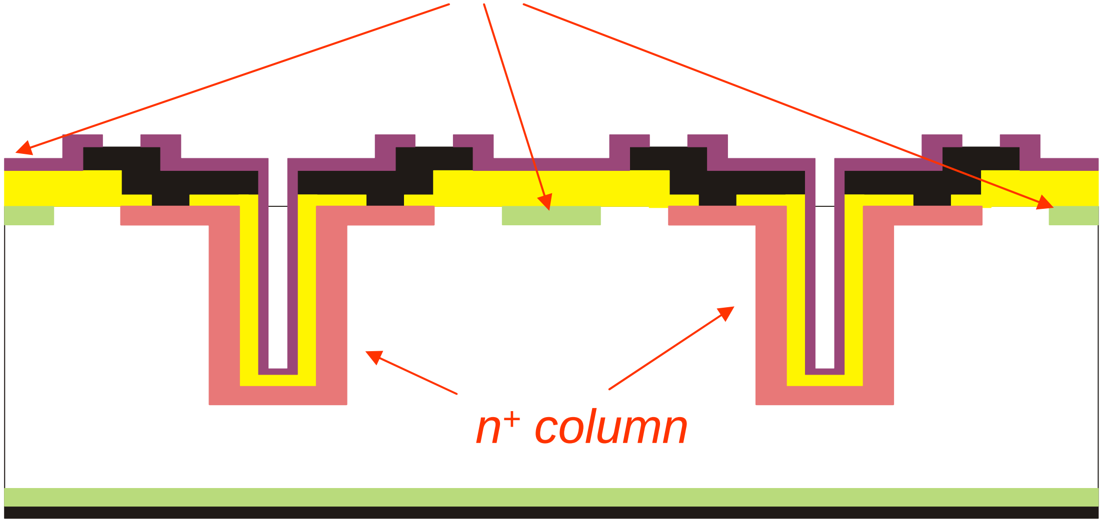
- Number of columns from 12000 to 15000
- Inter-columns pitch 80-100 μm
- Holes Ø 6 or 10 μm

3D process (1)

First Process

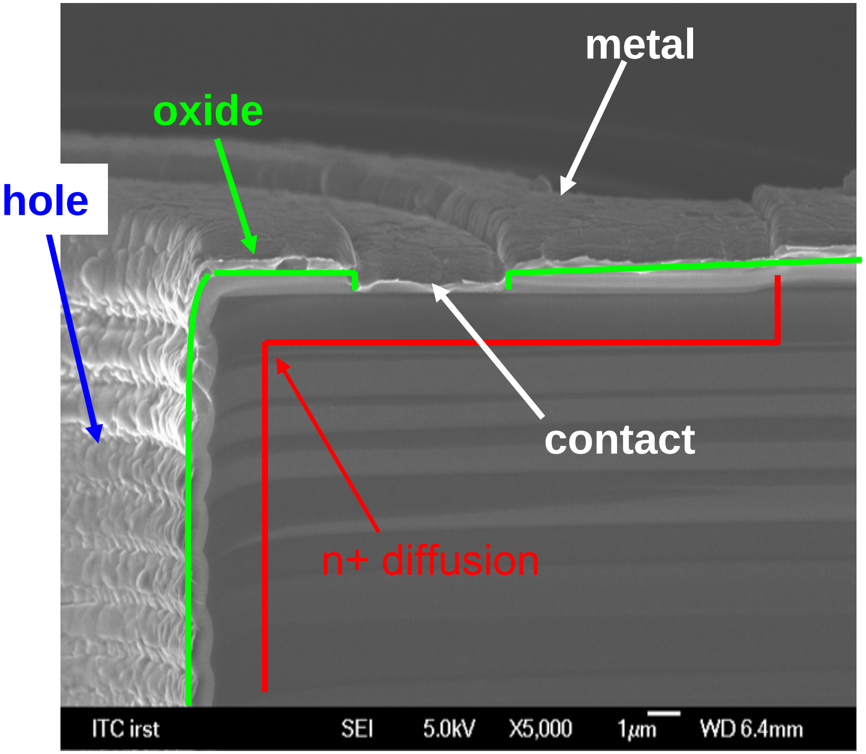
- p-type Si
- DRIE ~ 150µm
- no hole filling
- single column
- single side



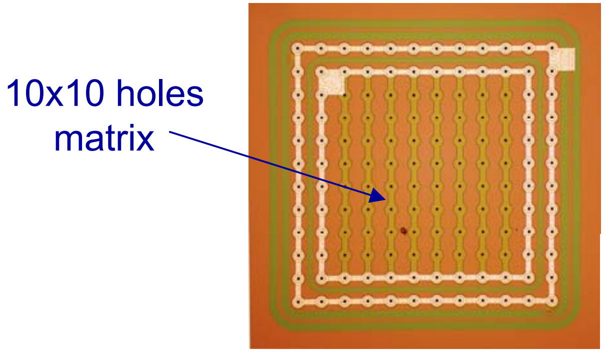


3D process (2)

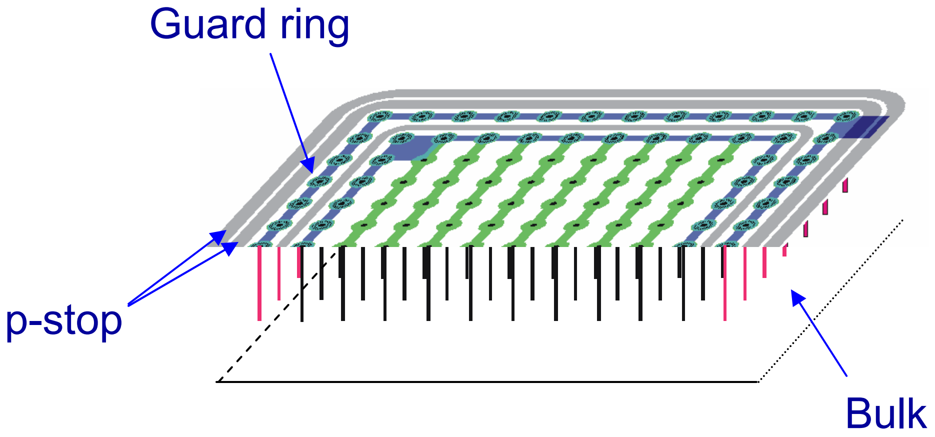
- ✓ Deep RIE performed at CNM, (we will have the D-RIE in IRST within this year)
- ✓ Wide superficial n+ diffusion around the hole to assure good contact
- ✓ No hole filling (with polysilicon)
- ✓ Passivation of holes with oxide
- ✓ Surface isolation: p-stop *or* p-spray



3D diode – layout:



10x10 holes matrix



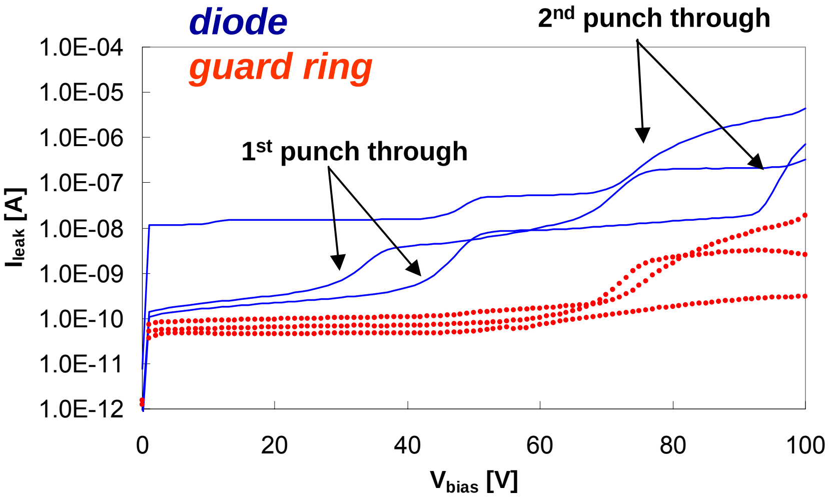
Guard ring

p-stop

Bulk

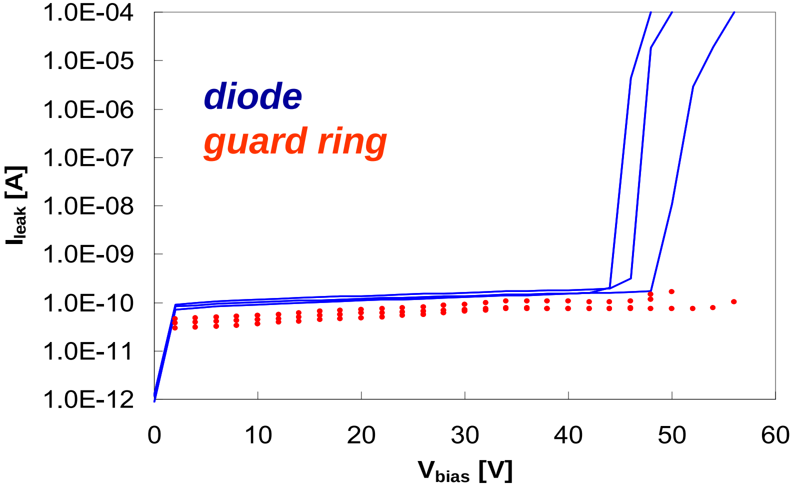
p-stop

Ileak = 0.68 ± 0.2 pA/column @ 20V

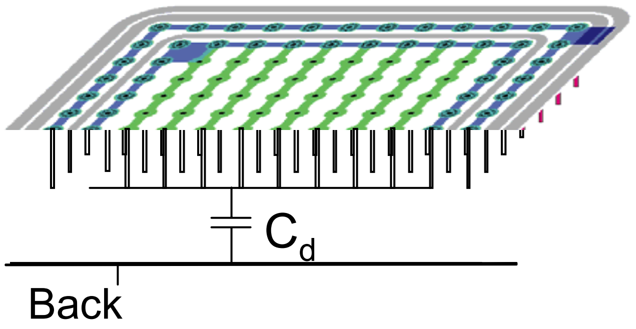


p-spray

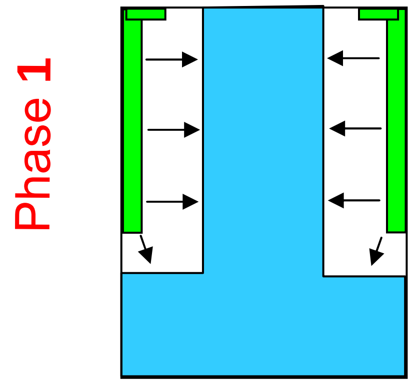
Ileak = 0.59 ± 0.12 pA/column @ 20V



3D diode – CV measurements p-stop



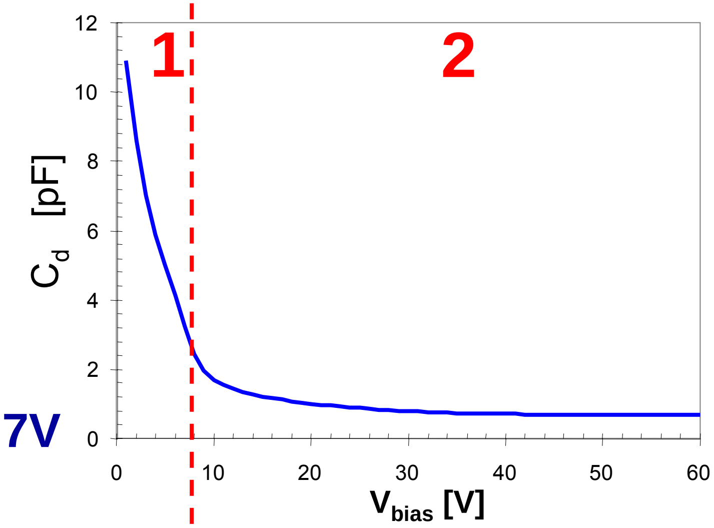
Capacitance measurement versus back on a 300µm thick wafer with ~150µm deep columns, 100µm picth

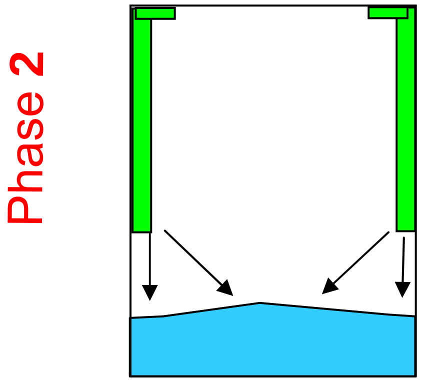


region between columns is not fully depleted

⇒ large capacitance

full dep. between columns ~ 7V

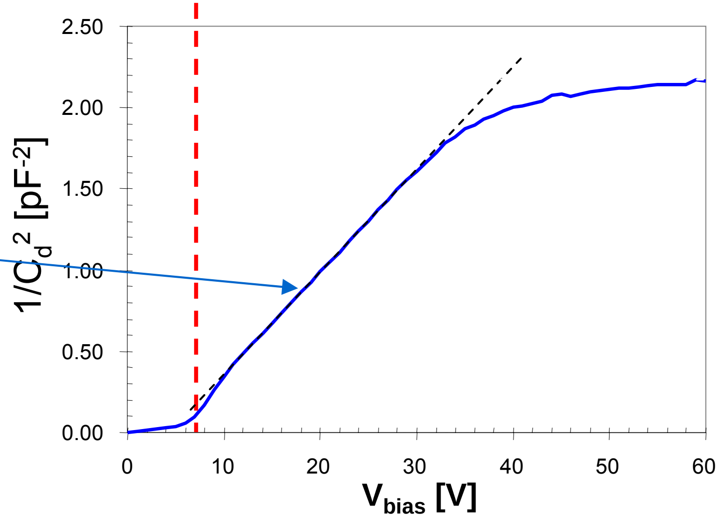




region between col. is fully depleted

⇒ depletion proceeds only towards the back *like a planar diode*

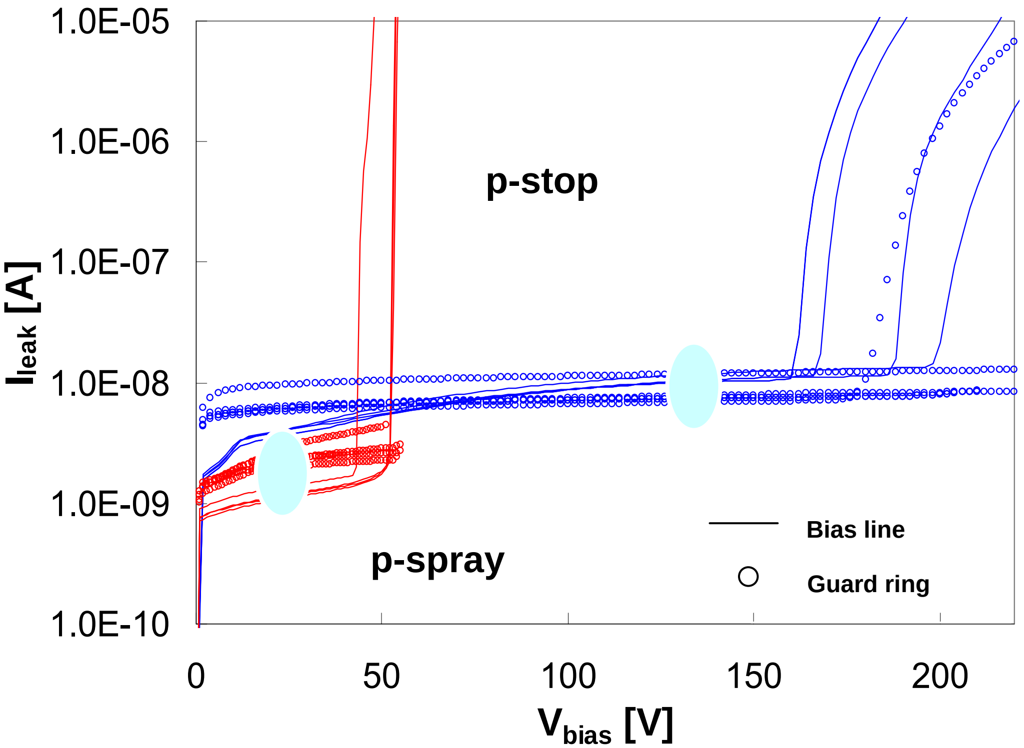
full depletion ~40V depletion width of ~150µm



Strip detectors electrical characterization

Electrical Chacaterization

- Leakage current: < 1pA/column
- Single-strip “backplane” capacitance: <5pF
- Inter-column capacitance range 12÷19 fF/column

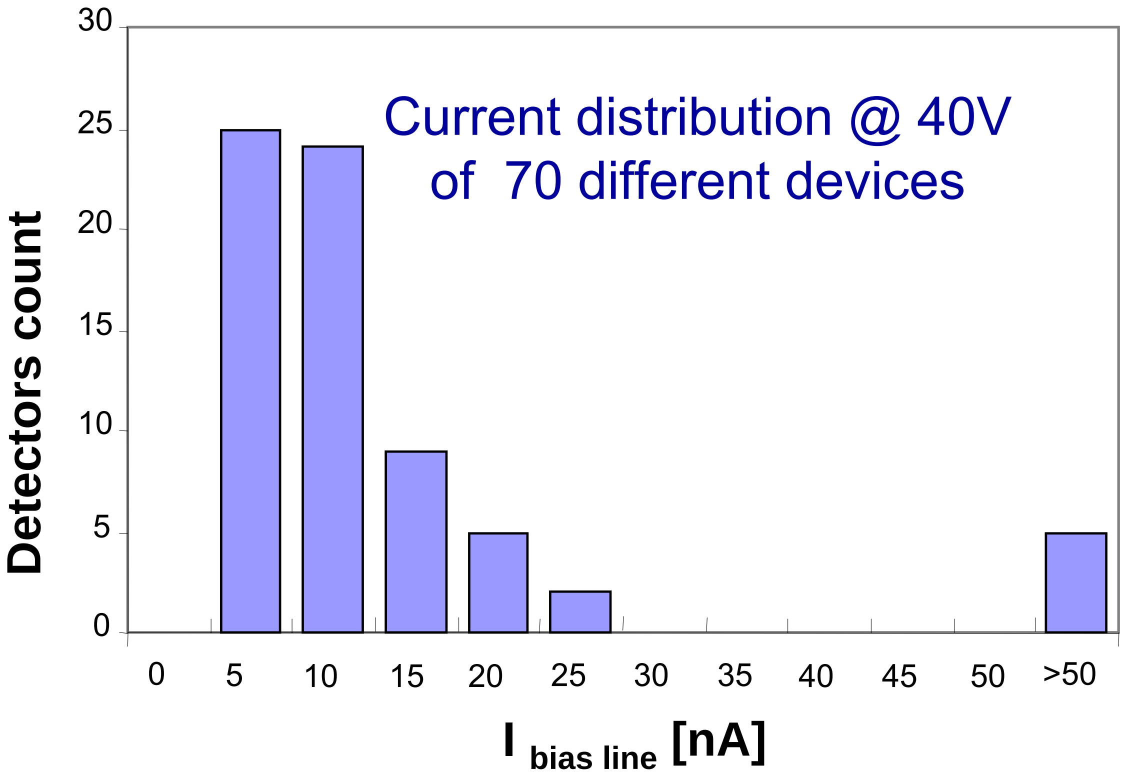


Number of columns per detector: 12000 - 15000

⇩

Average leakage Leakage current < 1pA/column

Strip detectors – IV measurements



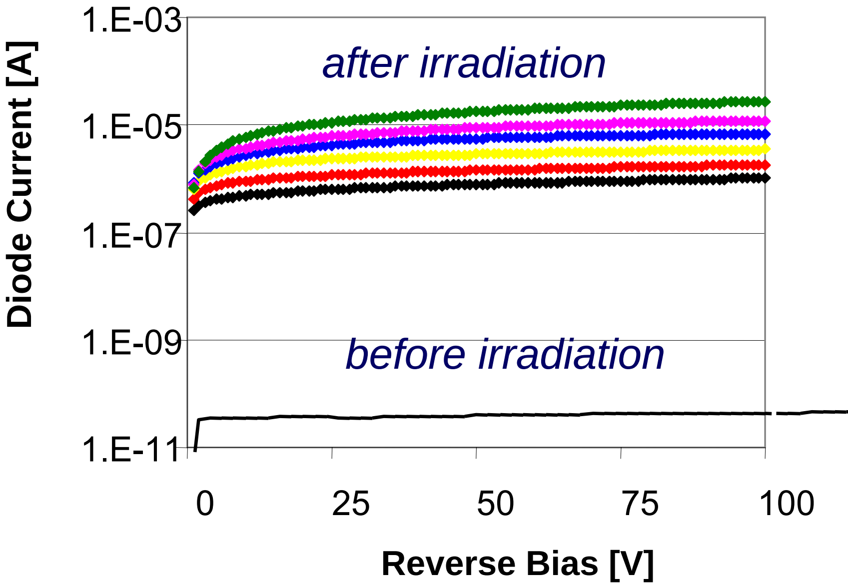
Good process yield

First production has proved the feasibility of 3D-stc detectors

on going activity

- ✓ University of Glasgow (UK): CCE measurements with α, β, γ on 3D diodes and short strips
- ✓ SCIPP (USA):
  CCE measurements on large strips
- ✓ INFN Florence (Italy): CCE meas with β,on 3D diodes;
- ✓ University of Freiburg (D);
  measurements on short strips
- ✓ Ljubljana:
  TCT and neutron irradiation

3D diode (80μm picth) irradiated at Liubliana at 5 different neutron fluences (from 5E13 to 5E15)

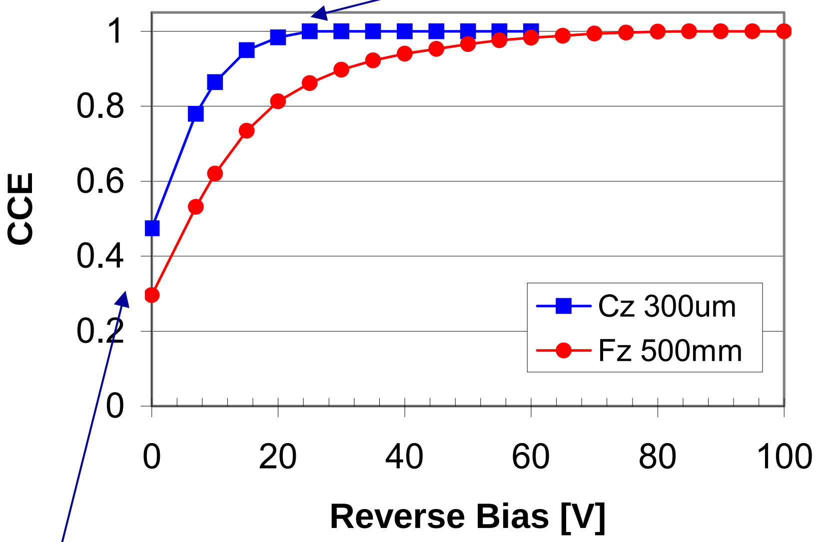


CCE measurements (preliminary)

Thanks to Carlo Tosi, Mara Bruzzi, Antonio De Sio
INFN and University of Florence

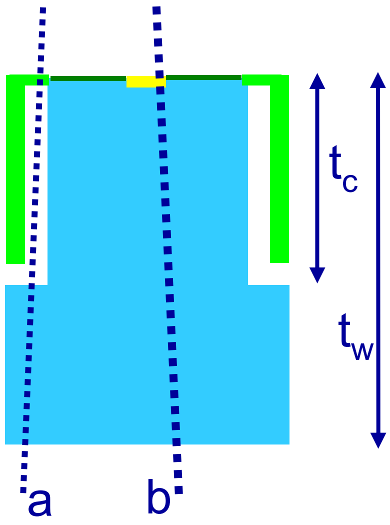
100% CCE @ low voltages

The fast reaching (before full depletion) of a 100% efficiency suggests that carriers generated in the undepleted region are effectively collected



CCE@0V ≈ t_c/t_w (for t_c ~ 150µm)

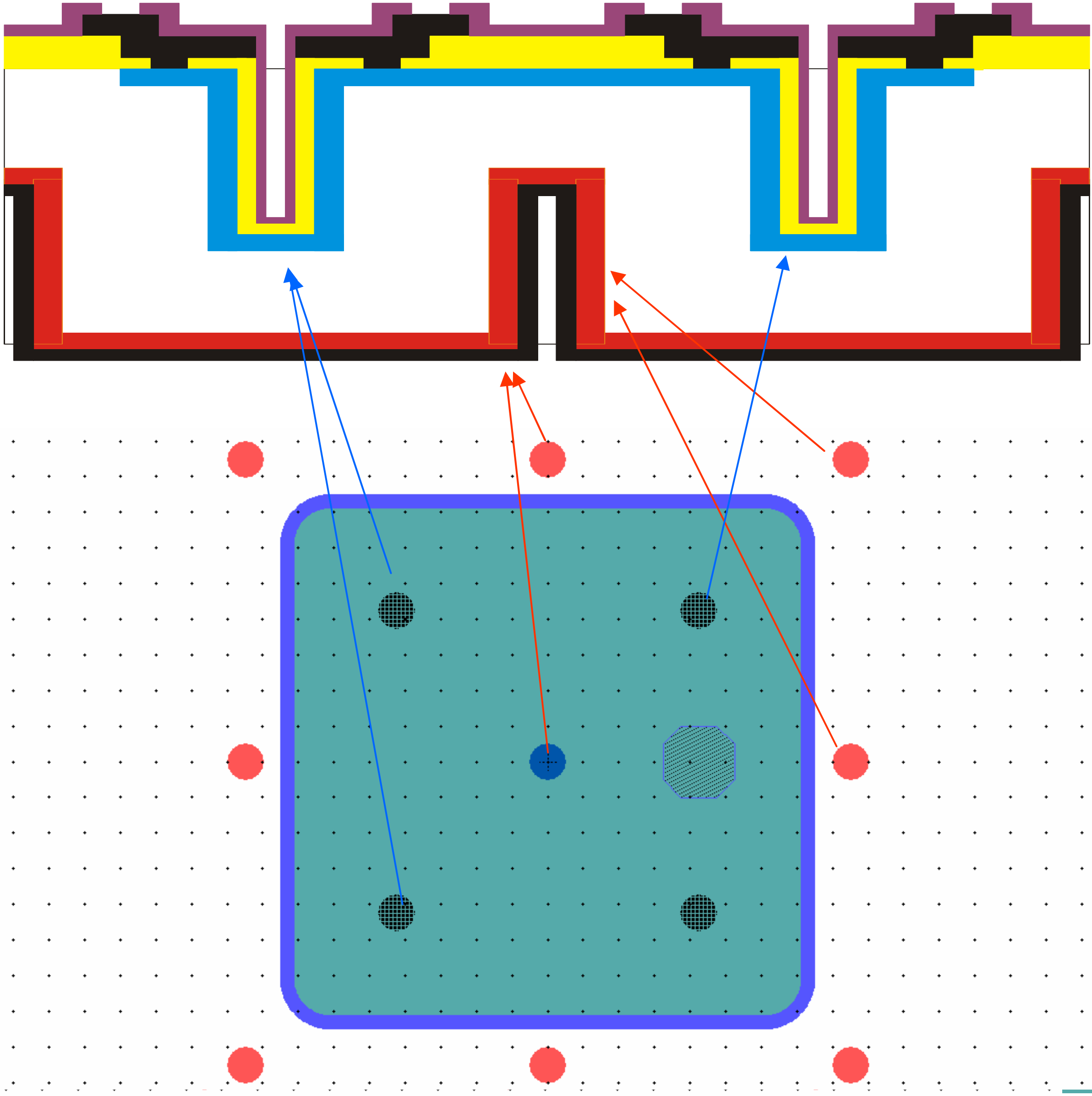
due to the peculiar geometry of 3D detectors, a region as deep as the column is always sensitive



Next Run

New Process

- n-type Si
- DRIE ~ 250mm
- no hole filling
- double columns
- double side



New Layout = Pixel

- MEDIPIX1
- ATLAS
- ALICE

3D Conclusion

First production has proved the feasibility of 3D-stc detectors

3D-stc detector:

- Advantage: “simple” fabrication process, extremely interesting device to tune the technology for the production of standard 3D detectors
- Disadvantage: in those applications not requiring charge information in short time Very long full charge collection times, can be used

Next Step:

- new process & new layout (pixel detector).

3D "technology"

3D active edge

- planar detector + dopant diffused in D-RIE etched edge then doped
 (C. Kenney 1997).

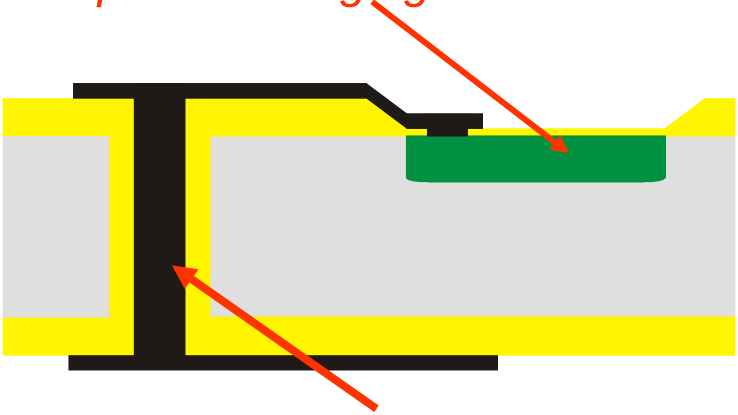
- Back plane physically extends at the edge.

- Active volume enclosed by an electrode: "active edge"

3D "readout technology"

- large area devices

- large area imaging systems


one pixel of imaging matrix

trench filled with doped polisilicon or metal

Imaging pixel matrices with 3D readout;
S. Eränen VTT finland

see at:http://tredi.itc.it/

Development of SiPM @ ITC-irst

SiPM – Outline

Introduction

- The Geiger-mode APD
- The Silicon PhotoMultiplier

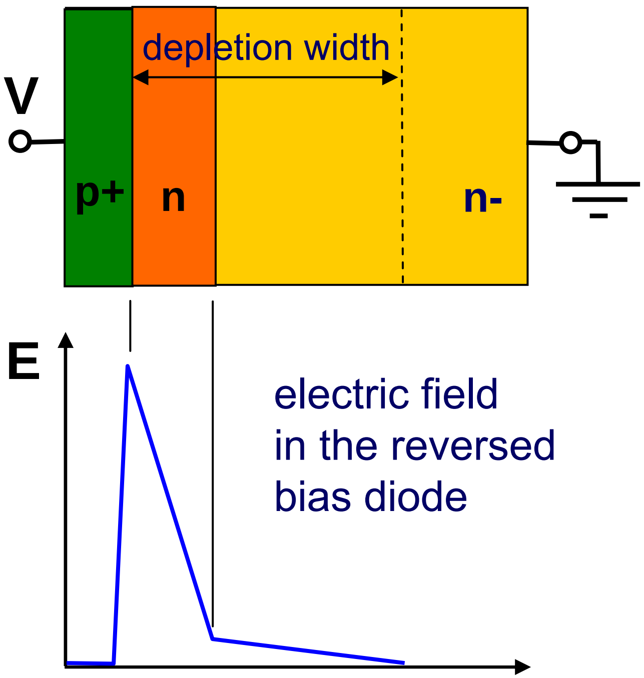
ITC-irst activity

- First results of the electrical characterization of the SiPMs produced at ITC-irst.

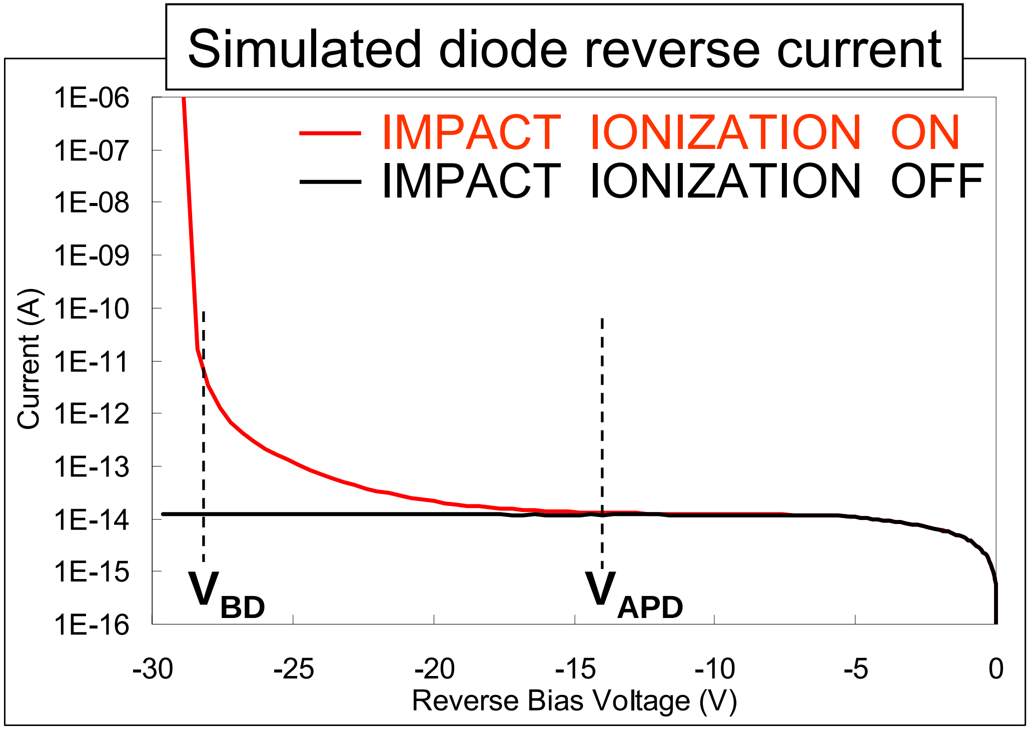
http://sipm.itc.it/

Impact Ionization

diode structure



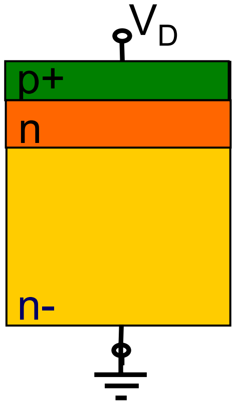
electric field in the reversed bias diode


Simulated diode reverse current

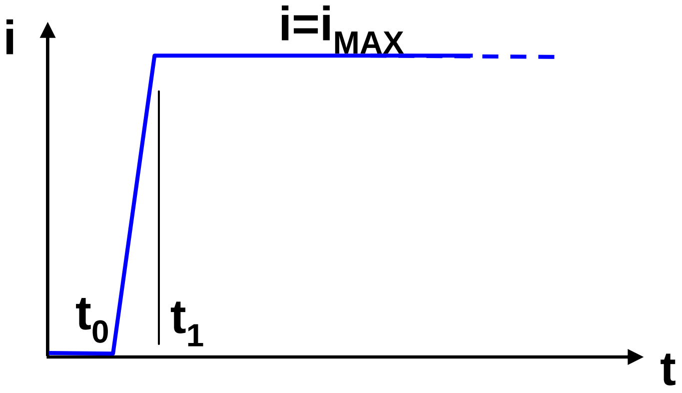
$V < V_{APD}$	=> photodiode	1 collected pair/generated pair
$V_{APD} < V < V_{BD}$	=> APD	<M> collected pairs/generated pair
$V > V_{BD}$	=> Geiger-mode APD	inf. collected pairs/generated pair

Geiger-mode APD

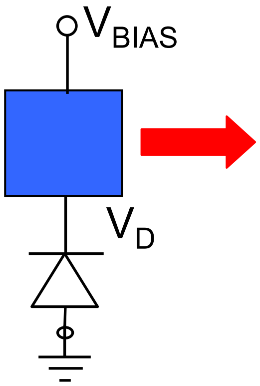
Diode biased at $V_D > V_{BD}$



$t < t_0$	i=0 (if no free carriers in the depletion region)
$t = t_0$	carrier initiates the avalanche
$t_0 < t < t_1$	avalanche spreading
$t > t_1$	self-sustaining current



In order to be able to detect another photon, quenching mechanism needed:



Two solutions:

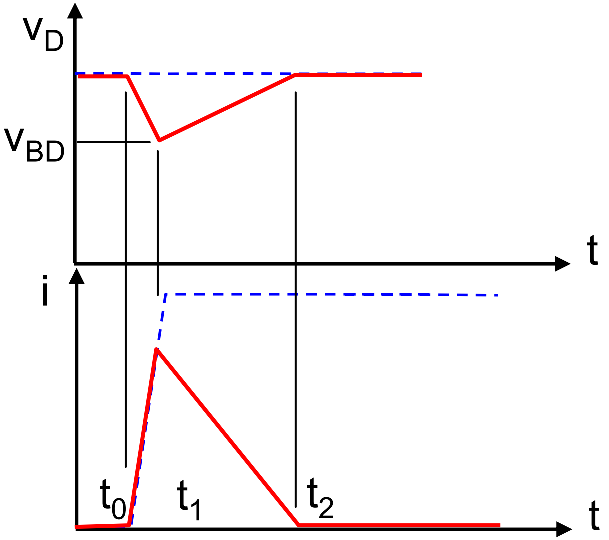
- large resistance:

  passive quenching

- analog circuit:

  active quenching

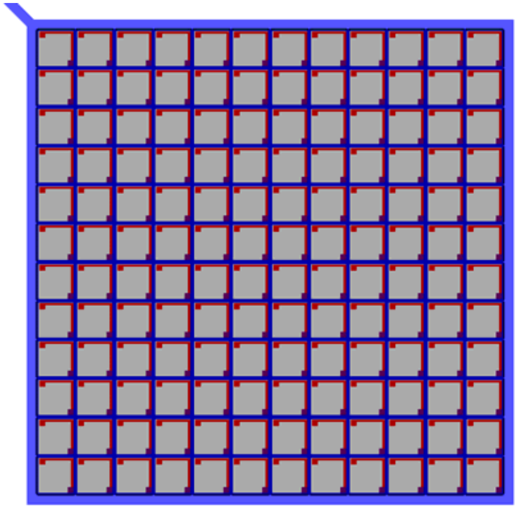
  [extended literature from politecnico di Milano (Cova et al.)]



SiPM concept

GM-APD gives no information on light intensity

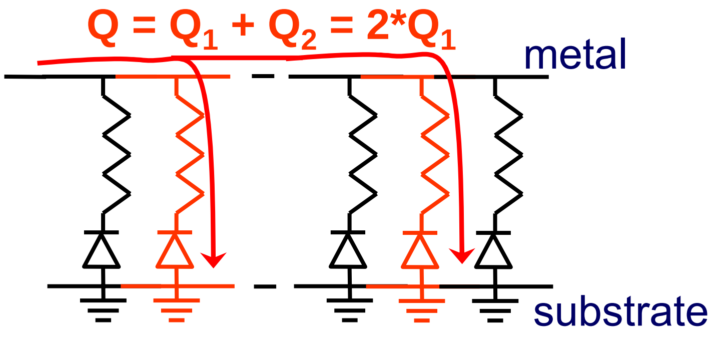
SiPM first proposed by Golovin and Sadygov in the mid '90



A single GM-APD is segmented in tiny microdiodes connected in parallel, each with the quenching resistance.

Each element is independent and gives the same signal when fired by a photon

⇒ output signal is proportional to the number of triggered cells that for PDE=1 is the number of photons



$Q = Q_1 + Q_2 = 2*Q_1$

Dark count

Noise = false counts triggered by non photogenerated carriers

Sources of free of carriers:

1. SRH generation in the depleted region
2. tunneling in high-field region
3. diffusion from the highly-doped regions

⇒ Dark count rate depends on:

- number of generation centres
- temperature
- overvoltage

Afterpulsing

AFTERPULSING: carriers are trapped during the avalanche and then released triggering an avalanche

If the carrier is released after the recovery time
=> increase dark count rate

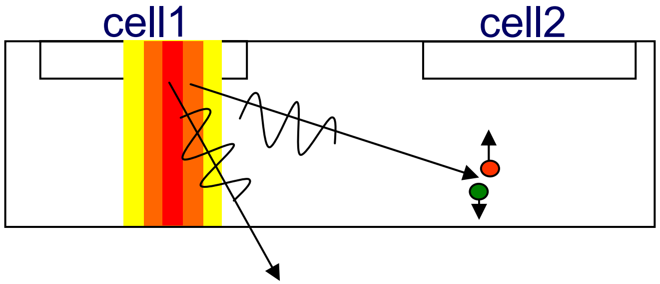
If it is released within the recovery time
=> no/smaller pulse

Afterpulse depends on:
- number of traps
- number of carriers transiting during an avalanche

=> Ideally the recovery time should be long enough so that the traps release the carrier within this time.

Optical cross-talk

During an avalanche discharge photons are emitted because of spontaneous direct carrier relaxation in the conduct. band



Those photons can trigger the avalanche in an adjacent cell: optical cross-talk.

Solutions:

- operate at low over-voltage => low gain => few photons emitted
- optical isolation structure:

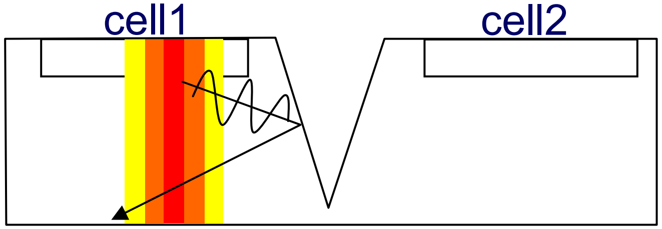
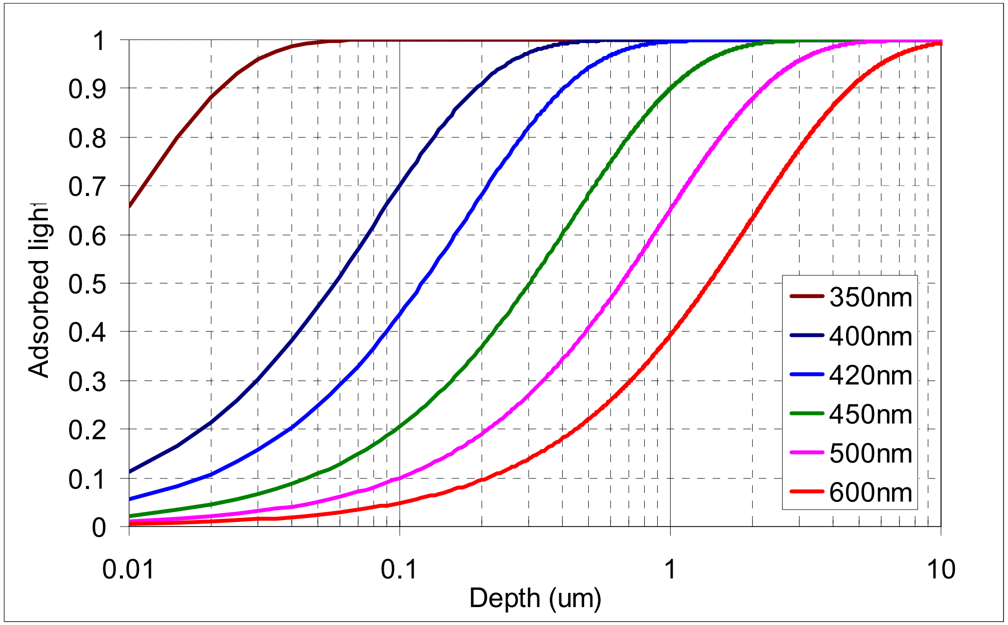


Photo-detection Efficiency

PDE = QE * Pt * Ae

1) Internal quantum efficiency



2) Transmission efficiency of the coating

Dead area is given by the structures at the edges of the microcell (metal layers, trenches, resistor…)

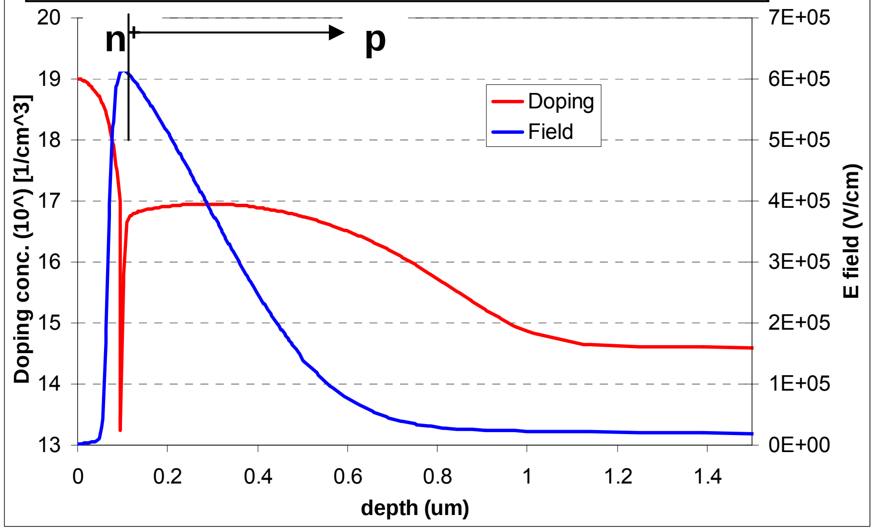
Electrons should trigger the avalanche because of the higher ionization rate

In any case, the higher the overvoltage is the higher Pt is.

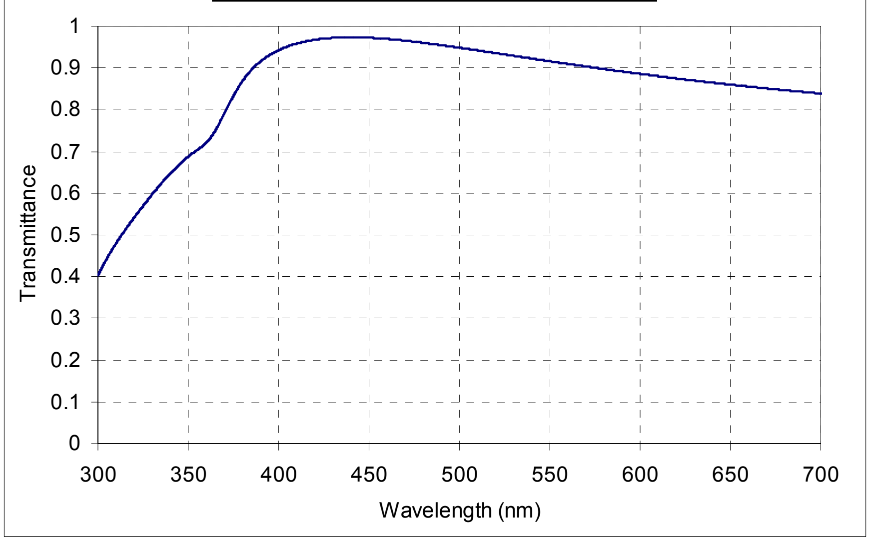
Characteristics of first prototypes

1. Substrate: p-type epitaxial
2. Very shallow junction to improve quantum efficiency at short wavelengths
3. Quenching resistance made of doped polysilicon
4. Anti-reflective coating optimized for λ~450nm
5. No structure for optical isolation
6. Geometry NOT optimized for maximum PDE

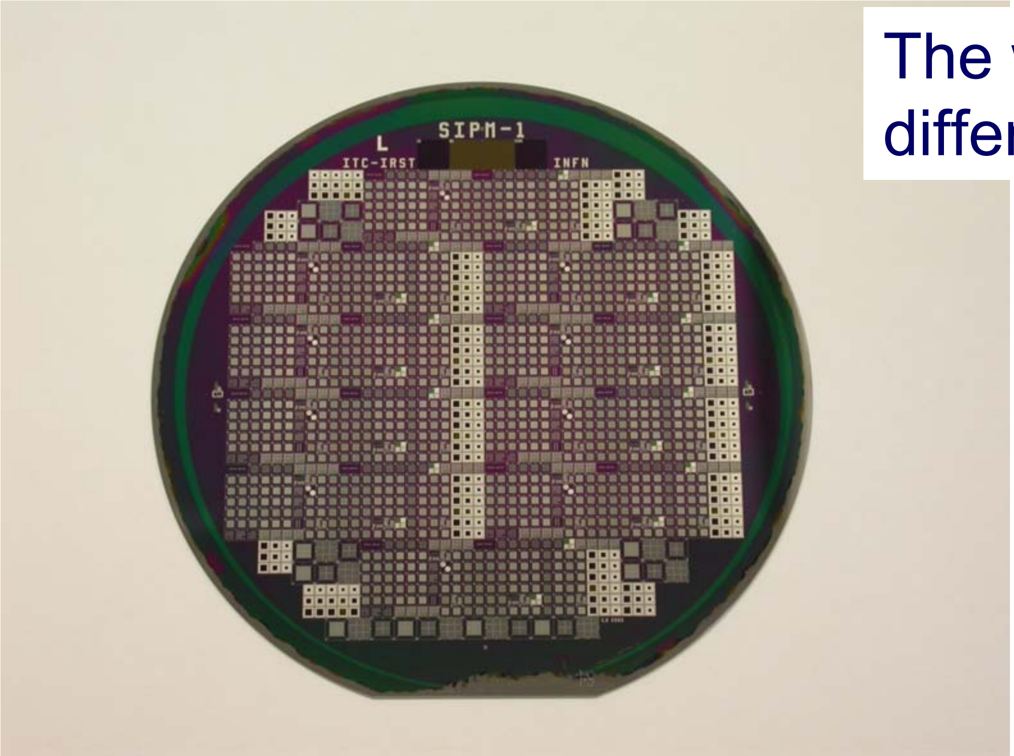
Doping profiles and Electric Field



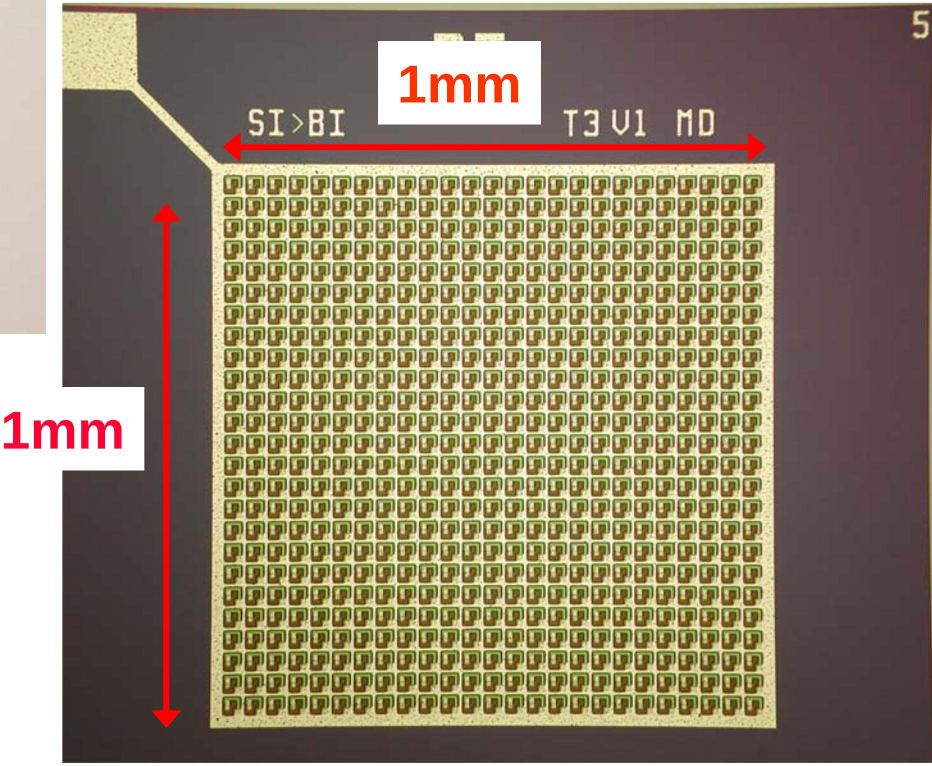
ARC transmittance



First prototypes



The wafer includes many structure differing in geometrical details

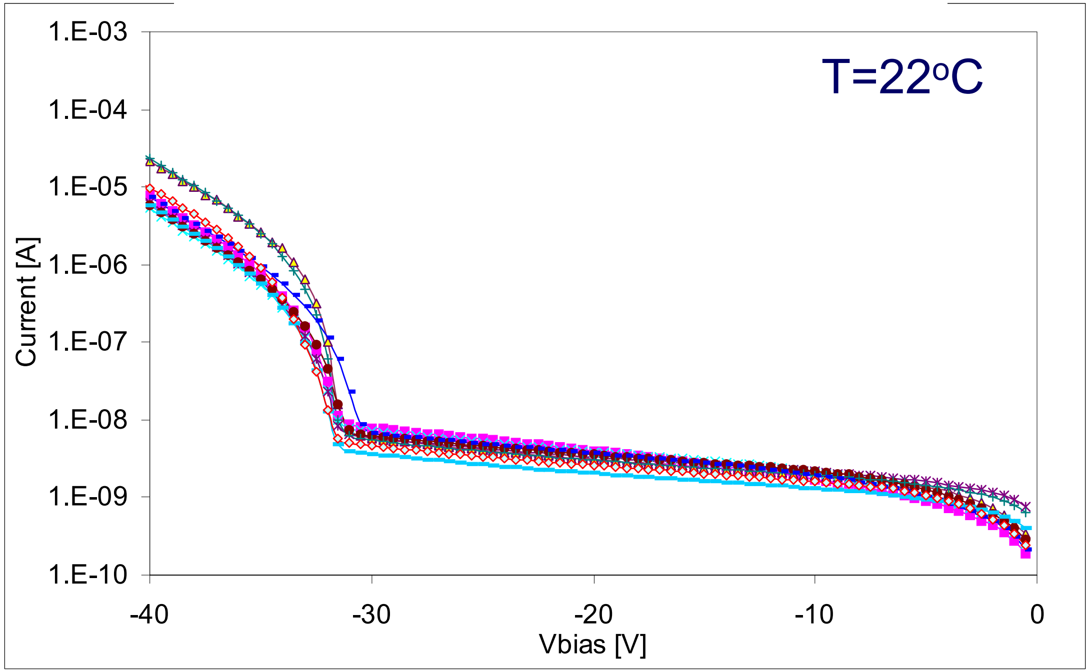


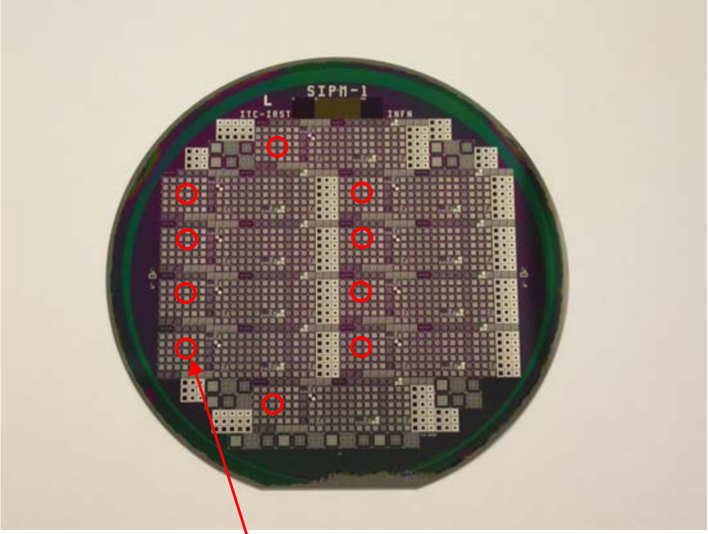
The basic SiPM geometry is composed by 25x25 cells

Cell size: $40 \times 40 \mu m^2$

Electrical characterization

IV characteristics of 10 devices





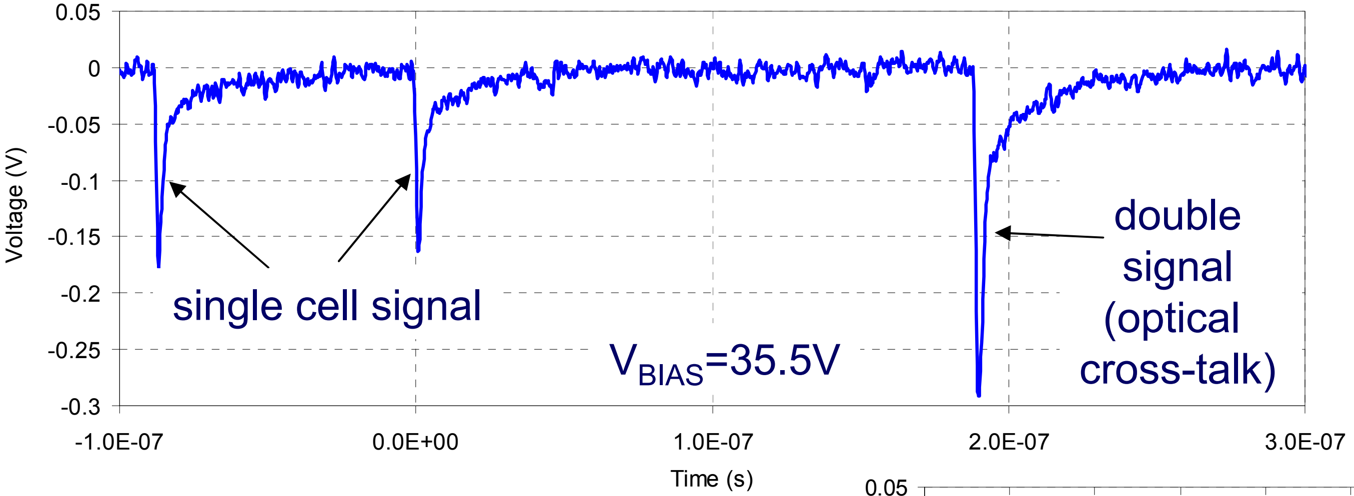
position of the devices

Messages from the IV curve:

- Breakdown voltage 31V. Uniform all over the wafer surface.
- post-breakdown current very uniform (measured on 90 devices) only 20% of the devices show anomalous behavior.

Signal characteristics

SiPM read-out by means of a wide-band voltage amplifier on a scope



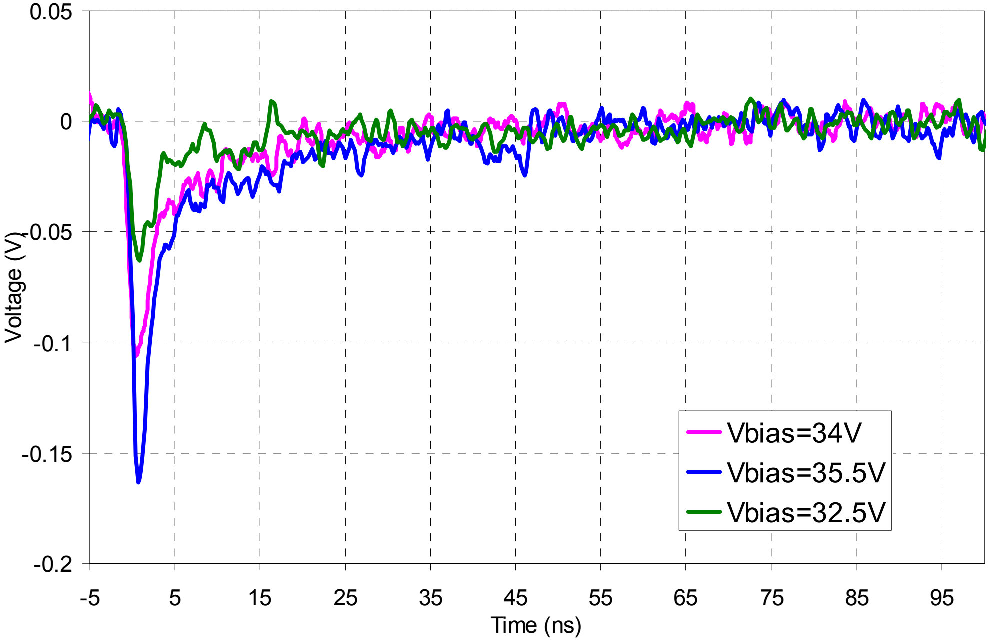
single cell signal

V_{BIAS}=35.5V

double signal (optical cross-talk)

Dark signal

T=22°C



Rise time ~1ns

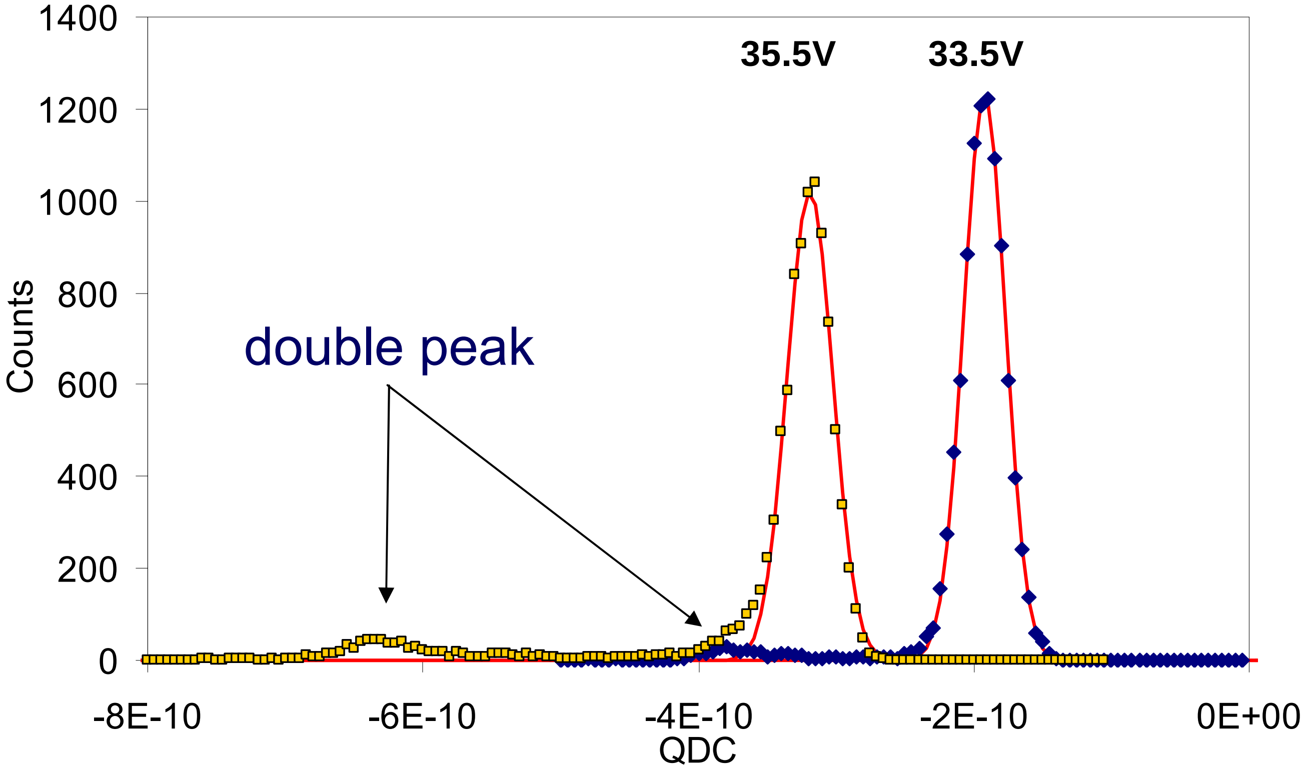
(limited by read-out system)

Recovery time ~70ns

Single electron spectrum

DARK

Single electron spectrum in dark condition
Integration time = 10ns.

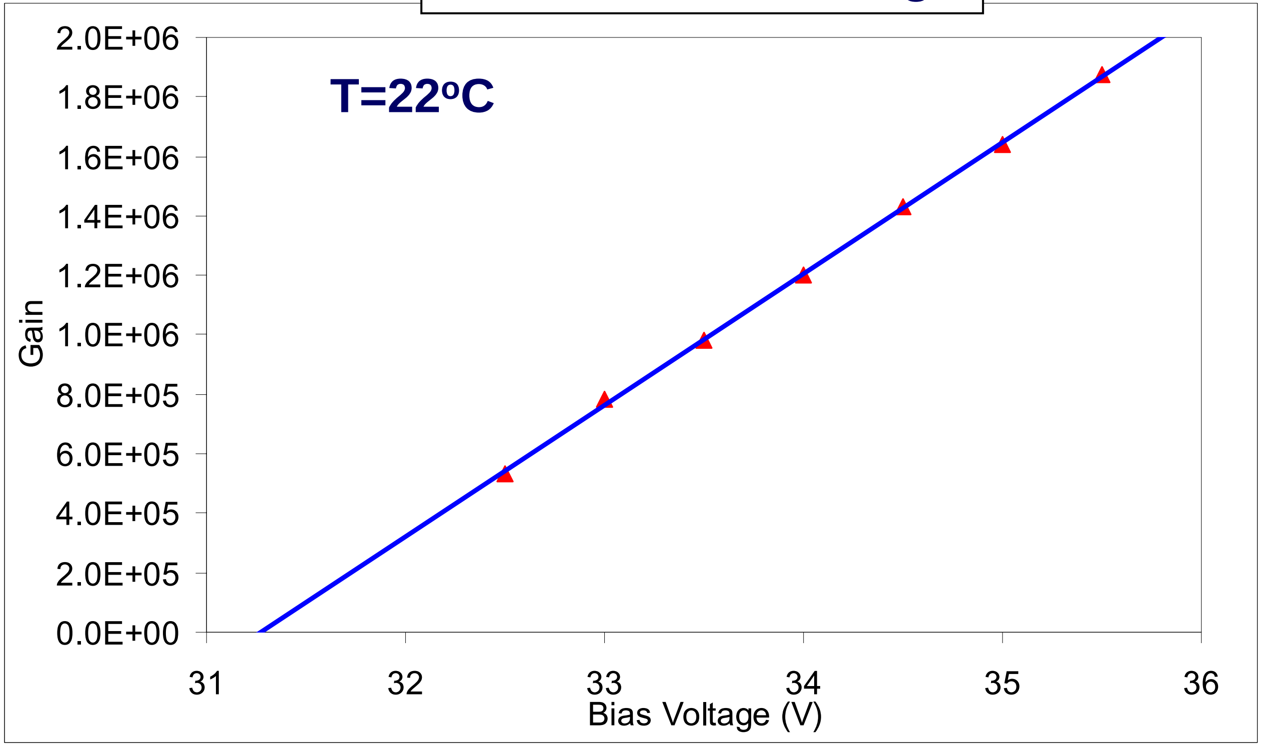


For V_{BIAS}=35.5V double peak counts = 1/20 single peak counts

Gain

DARK

Gain *vs* Bias voltage

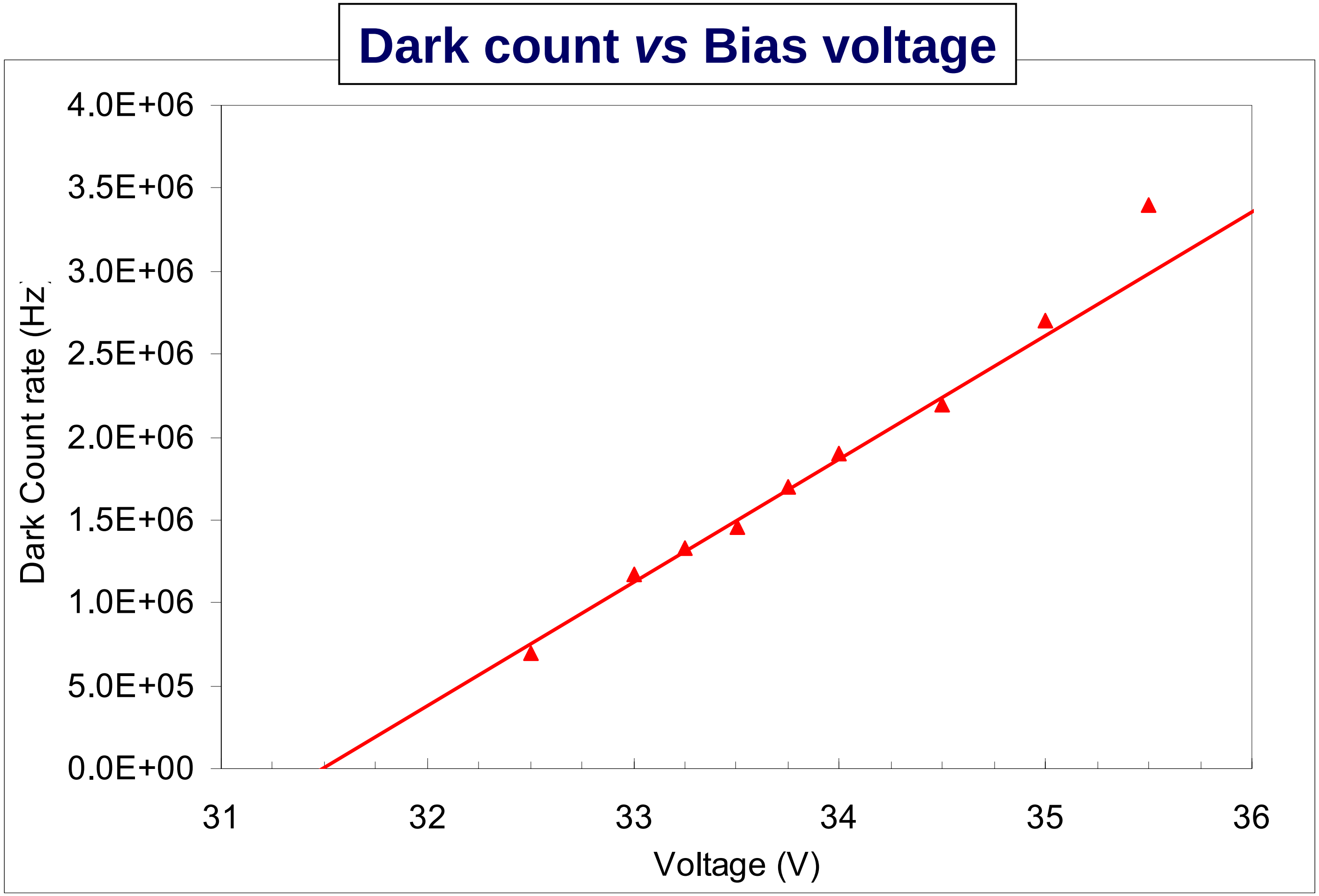


Linear dependence, as expected.

$Q=C_{microcell}*(V_{bias}-V_{breakdown})$

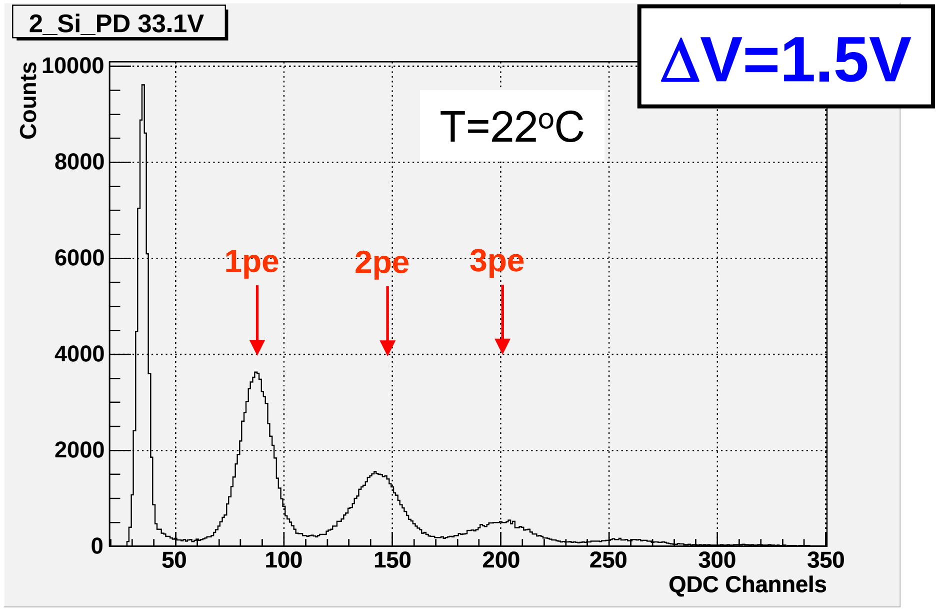
=> C = 80-90fF

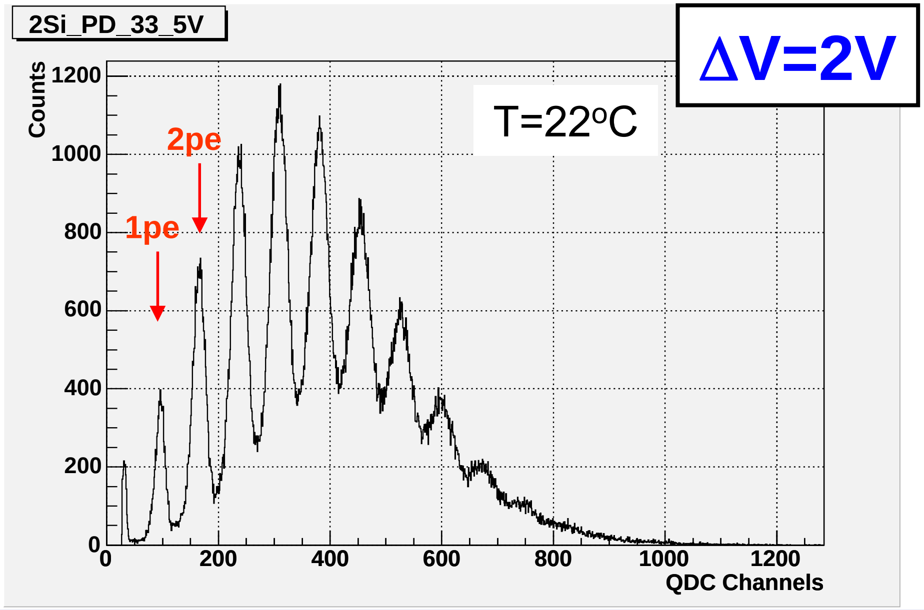
Dark count


Dark count *vs* Bias voltage

Dark count increases linearly with voltage.
=> PDE should follow the same trend.

Response to light





Pulse charge spectrum from low-intensity light flashes (red LED)

Each peak corresponds to
a different number of fired cells

Very good uniformity response from the micro-cells

Energy resolution

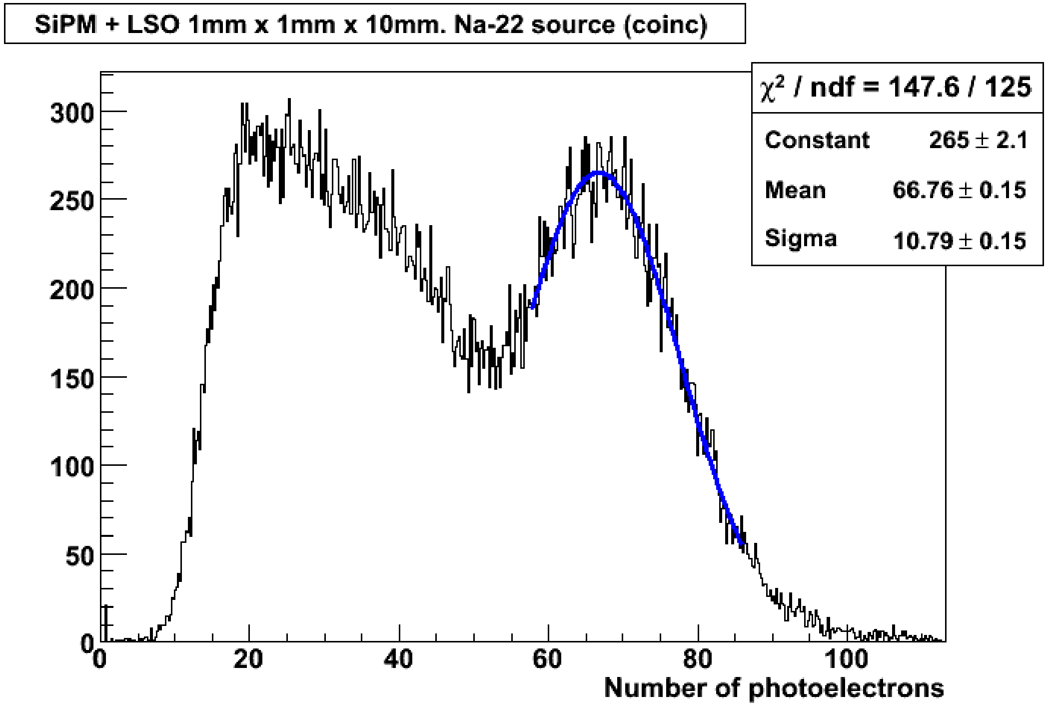
VERY PRELIMINARY from Pisa (A. Del Guerra)

Very first measurement on one single device

- 1mmx1mmx10mm **LSO crystal coupled to a SiPM**
- Data taken in coincidence with a 10mm diam, 5mm thick YAP crystal coupled to a PMT.
- ^{22}Na source.
- 2.5V overvoltage
- **37% energy resolution**

1) Optimizing the set-up and the working conditions this value can be improved

2) Area efficiency has to be optimized yet!


SiPM + LSO 1mm x 1mm x 10mm. Na-22 source (coinc)

SiPM Conclusion

- **Extremely encouraging results from the first production of SiPMs at ITC-irst.** Fully functional devices with:
  - Gain ~ 10^6 (linear with V_{BIAS})
  - Dark count ~ MHz
  - Recovery time ~ 70ns
  - Good uniformity of the micro-pixels response
  - PDE measurement in progress, encouraging first results
- **Second production run just completed.**
  - Implemented trenches for optical cross-talk isolation.
  - As for the first run, IV measurements indicate a high production yield (80%)
- **Next steps**: SiPMs with lower dark count

Acknowledgements:

Thank to all the people involved in the ITC-irst & INFN project DASIPM and TREDI

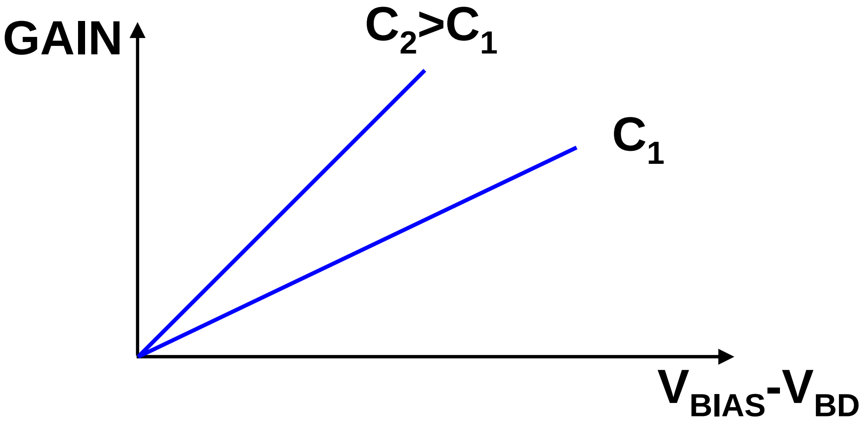
		VACUUM TECHNOLOGY			**SOLID-STATE TECHNOLOGY**		
		PMT	**MCP-PMT**	**HPD**	**PN, PIN**	**APD**	**GM-APD**
Photon detection efficiency	**Blue**	20 %	20 %	20 %	60 %	50 %	30%
	Green-yellow	40 %	40 %	40 %	80-90 %	60-70 %	50%
	Red	< 6 %	< 6 %	< 6 %	90-100 %	80 %	40%
Timing / 10 ph.e		~ 100 ps	~ 10 ps	~ 100 ps	tens ns	few ns	tens of ps
Gain		$10^6 - 10^7$	$10^6 - 10^7$	$3 - 8x10^3$	1	~ 200	$10^5 - 10^6$
Operation voltage		1 kV	3 kV	20 kV	10-100V	100-500V	< 100 V
Operation in the magnetic field		$< 10^{-3}$ T	Axial magnetic field ~ 2 T	Axial magnetic field ~ 4 T	No sensitivity	No sensitivity	No sensitivity
Threshold sensitivity (S/N>>1)		1 ph.e	1 ph.e	1 ph.e	~100 ph.e	~10 ph.e	~1 ph.e
Shape characteristics		sensible bulky	compact	sensible, bulky	robust, compact, mechanically rugged		

GAIN

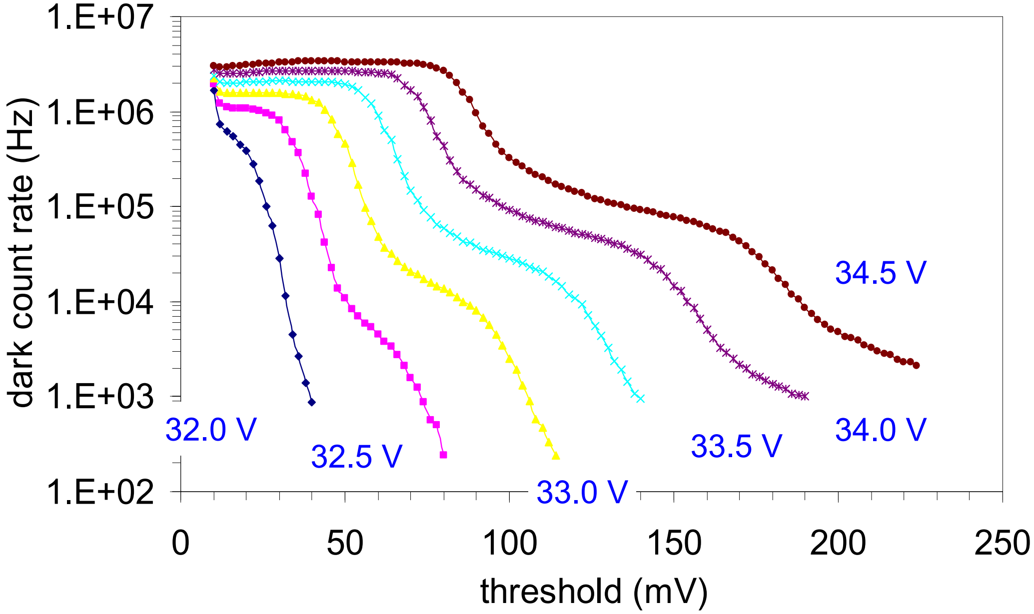
The area of the current pulse represents the gain

$$\mathbf{GAIN} = \mathrm{Area}/q = I_{MAX} \times \tau / q = \mathbf{C \times (V_{BIAS}\text{-}V_{BD})/q}$$

The capacitance should be large in order to have a high gain.
On the other hand, a large capacitance leads to longer recovery times.



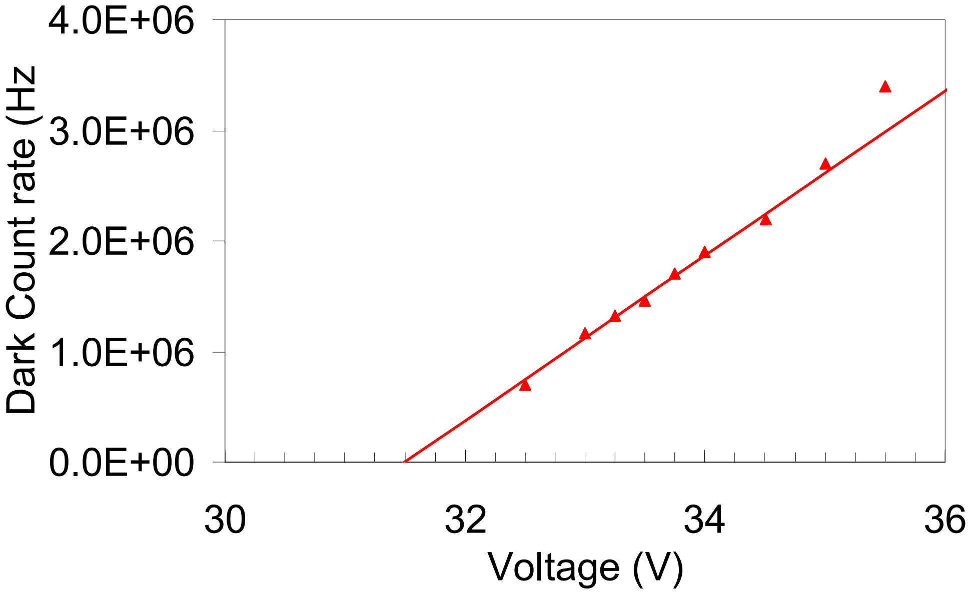
SiPM dark count



Room temperature (~ 23°C)
- 1 p.e. dark count rate: ~ 3 MHz
- 3 p.e. dark count rate: ~ 1 kHz

trenches for the optical isolation between micro-cells were not implemented in the first run

Dark count rate:
- linear variable with V_{bias}
- increases with the temperature

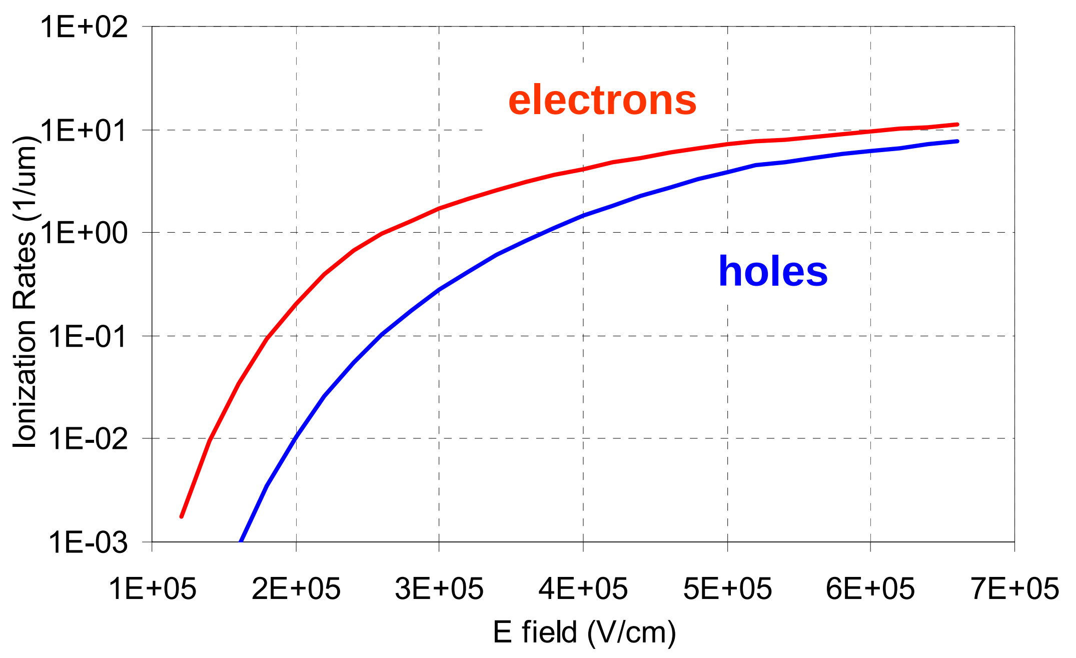


Turn-on probability

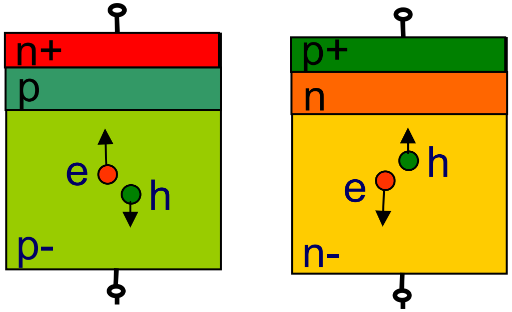
P_{01} = turn-on probability = probability that a carrier traversing the high-field region triggers the avalanche.

⇒ it affects the detection efficiency!

It is linked to the ionization rates.



1) electrons higher ioniz. rate



⇒ first solution is better

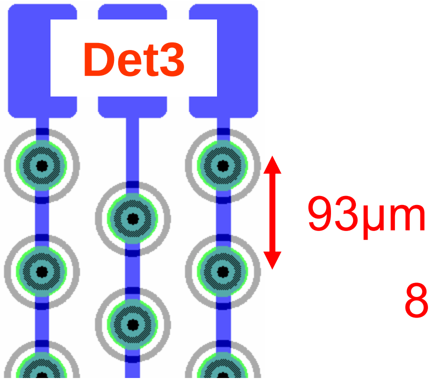
2) ioniz. rates increase with field

⇒ **increased probability for higher over-biasing**

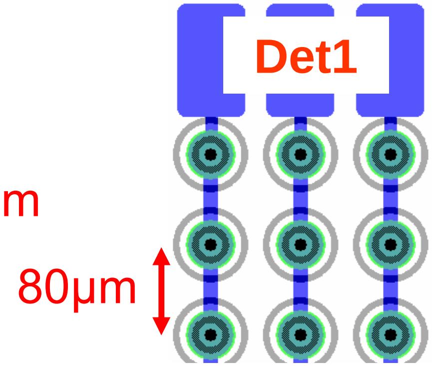
Strip detectors – CV measurements

Capacitance measurement between one strip and the two first neighboring

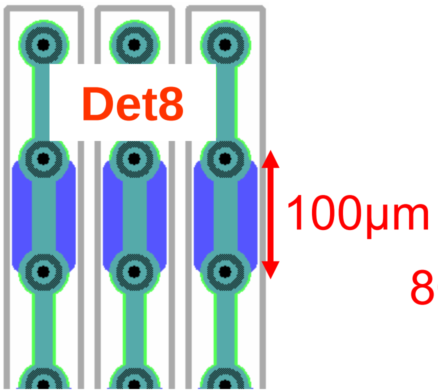
p-stop; DC coupling; strip pitch=80µm



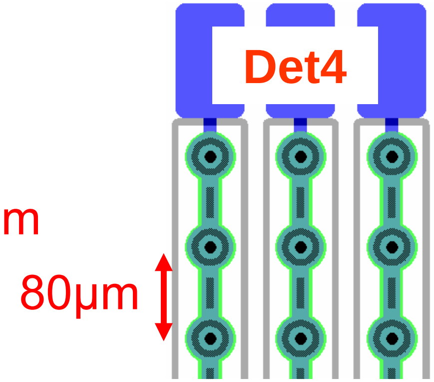
196 columns per strip



230 columns per strip

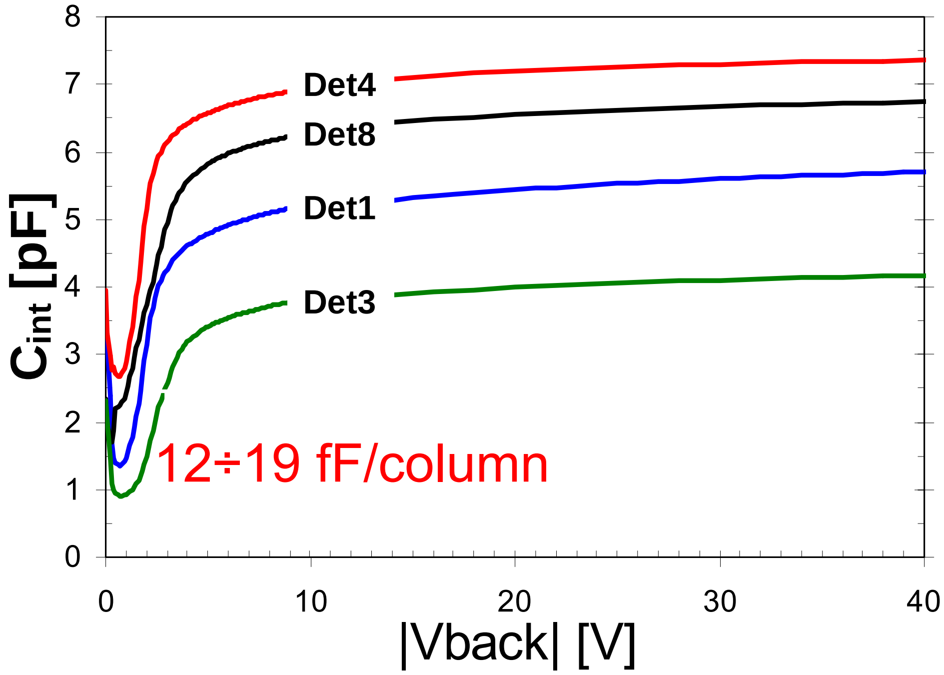


184 columns per strip



230 columns per strip

f=100kHz



12÷19 fF/column

Other capacitance measurement results

Typical single-strip “backplane” capacitance (after lateral full depletion)
<5pF (~200 columns)

Typical coupling capacitance for AC detectors ~ 60pF

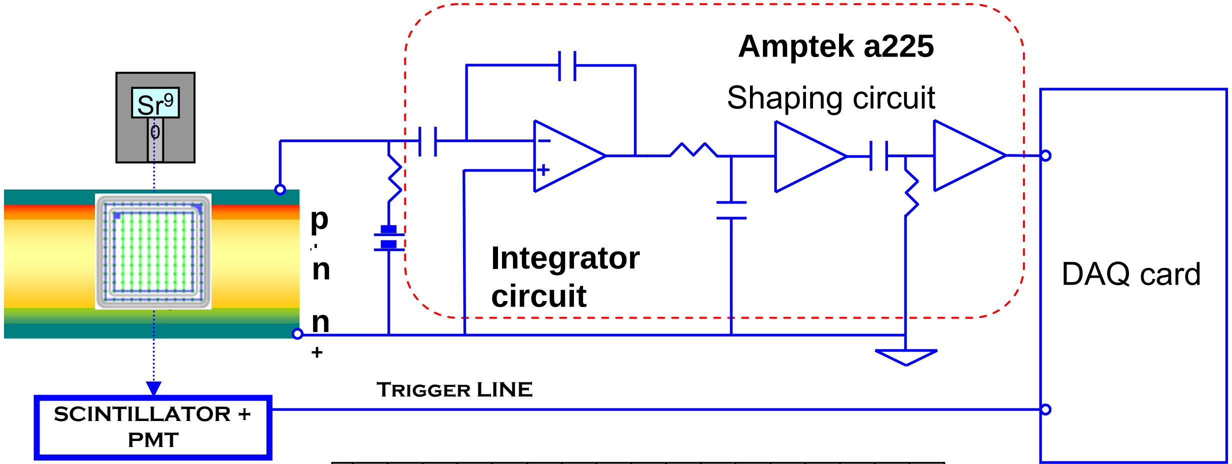
3D diode – CCE measurements

(preliminary)

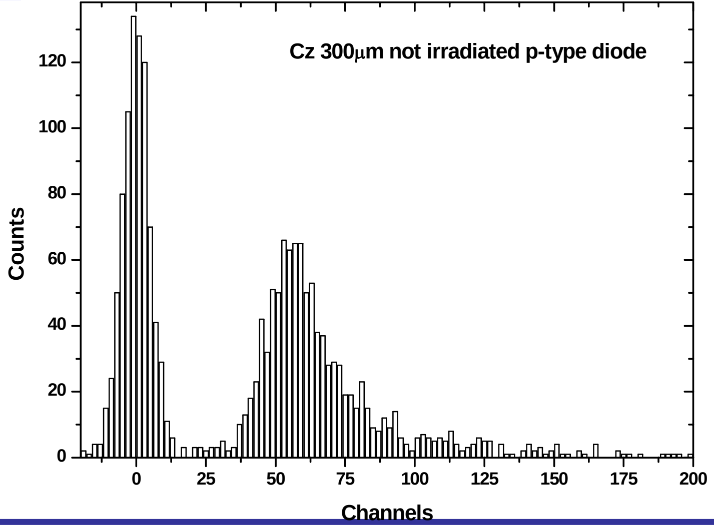
Carlo Tosi, Mara Bruzzi, Antonio De Sio
INFN and University of Florence

Original system:
β^- source
Shaping time: 2.4μs
ENC= (280+5.6C/pF)e$^-$
Max inverse current= 1500pA

Actual System:
Max inverse current=10μA
Noise=2000e$^-$



Calibration on Cz, 300μm, p-type planar diode


Cz 300μm not irradiated p-type diode