Fast Neutron Irradiation of Monolithic Active Pixels Sensors dedicated to particle detection

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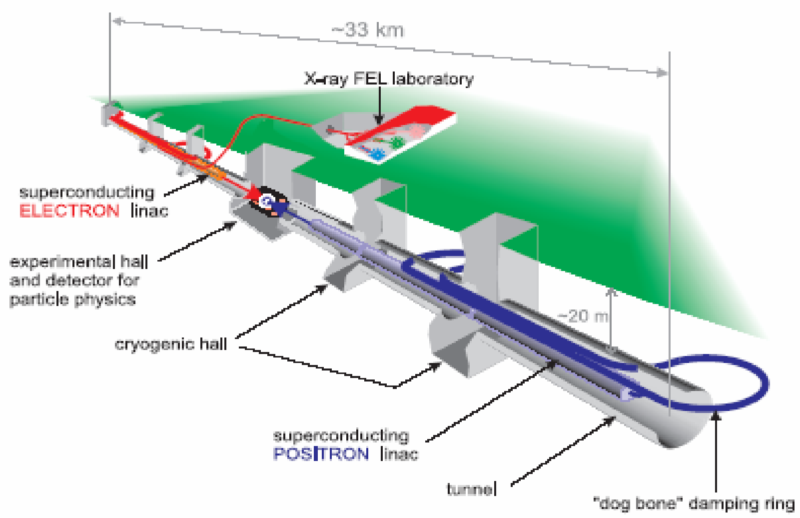
The International Linear Collider

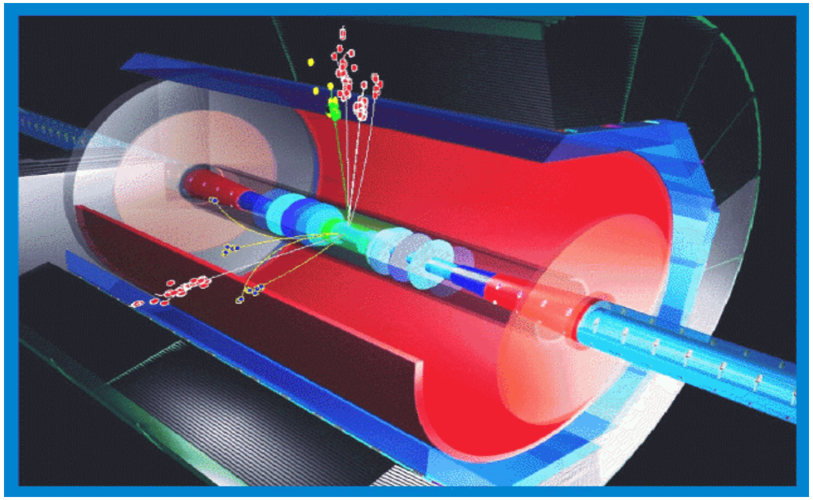
- **The LHC will be a machine dedicated to basic discoveries**
- **The electron-positron International Linear Collider may allow precision measurements if commissionned**



Physics:

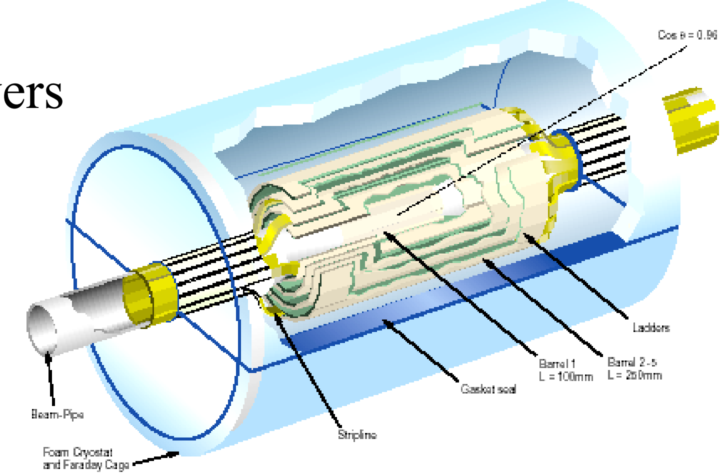
- Higgs mechanism
- Supersymmetry (SUSY)
- Extra dimensions

Precision measurements require tracking and vertexing with improved resolution



Challenges for the vertex detector

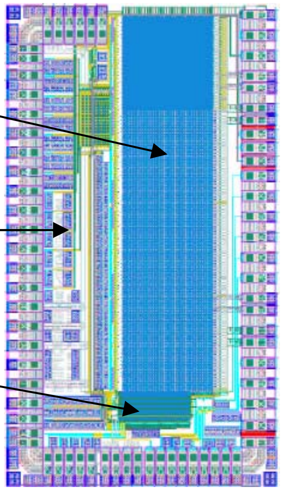
- 5 layers of pixels: very compact
  Inner layer = 1,5cm radius (very close to the beam) , Outer layer = 6cm
- Very good spatial resolution ≤ 5µm
- High Detection efficiency ~ 99%
- High granularity
  - Pixel width ~20x20 µm^2 (for the first layer)
  - Total of ~ 500 million pixels for the 5 layers
  (2 to 3 orders of magnitude higher than present experiments !!!)



- Very fast readout
  - 25 µs => 1st layer,50 µs => 2nd layer
  - 200-250 µs => 3rd to 5th layers
- Radiation tolerance
  - Displacement damage ~ 10^{10} neutrons (1 MeV equivalent)/cm^2.year
  Ionizing irradiation: 50 kRad/year ***(much lower than for the LHC….)***

➡ MODERATE COST !!!

MIMOSA8/HiMAPS-1 chip



32 x 128 pixels

- **Minimum Ionizing Particle MOS Active Pixel Sensor**
- **High Speed Monolithic Active Pixel Sensor**

- Chip fabricated with TSMC 0.25µm digital process

The chip in details:

4 pixel designs 25µm x 25µm

S1 Strasbourg design

S2, S3, S4 Saclay design

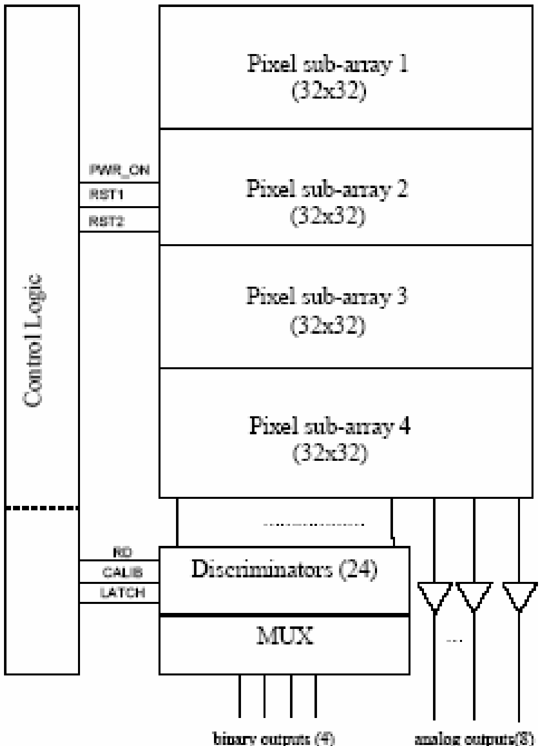
GOALS

⇨ **Pixel level CDS**

analog and digital outputs

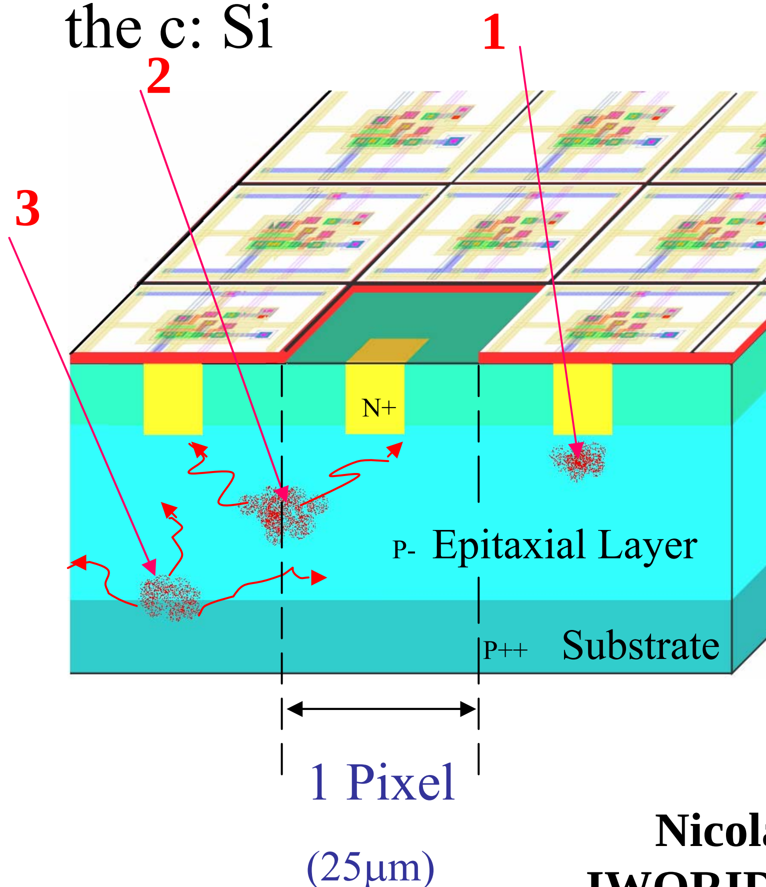
⇨ **Fast readout**

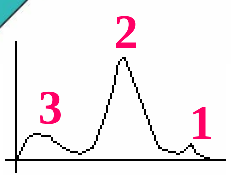
→ up to 20µs for the analog and digital readout



Analog outputs characterization

Source : (^{55}Fe → X rays) which interact with electrons of the c: Si





1) The electrical charge is collected almost entirely by the n-well of a single pixel. The signal is maximum and induces a **calibration peak (1).**

2) The electrical charge is split into two contributions. It is collected by two or more pixels. This gives rise to a medium energy peak (2).

3) Part of the charge is lost in the substrate-some charge is collected by few close diodes. This is responsible for the low energy background (3).

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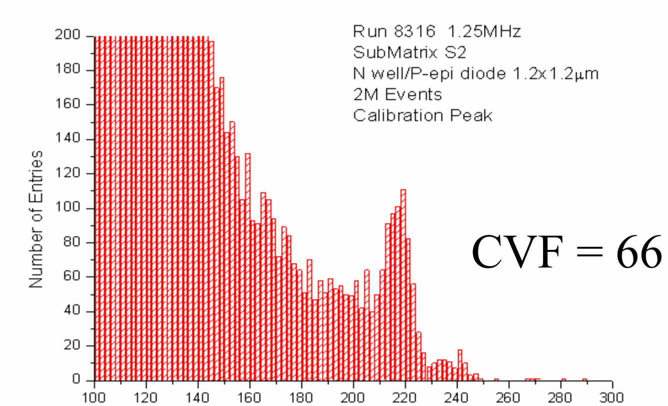
Analog outputs

We observe a calibration peak for which almost 100 % of the charge is collected by one single pixel. With realistic assumptions the conversion factor (CVF) may be deduced.

S2

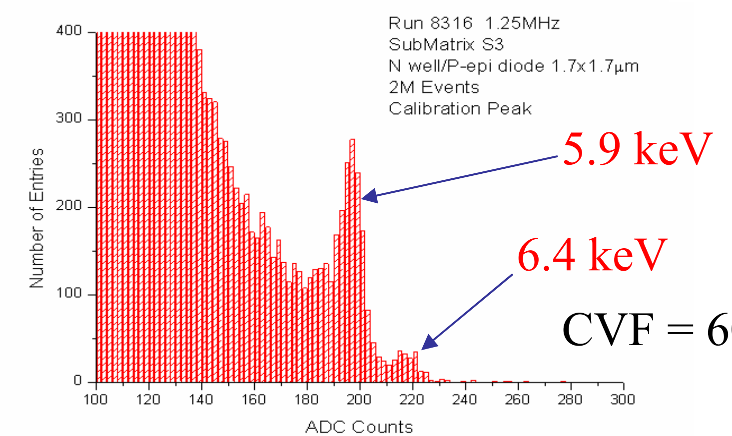


CVF = 66 μv/e-

Clock frequency F = 1.25MHz,
2M events

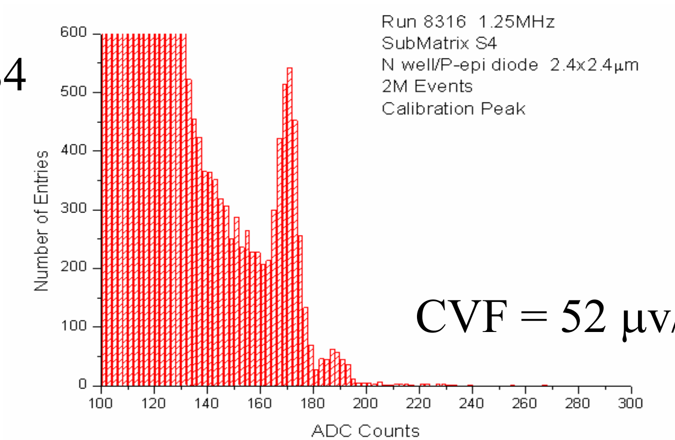
(1 UADC = 0.5mV)

S3



CVF = 60 μv/e-

S4



CVF = 52 μv/e-

Analog outputs

Summary

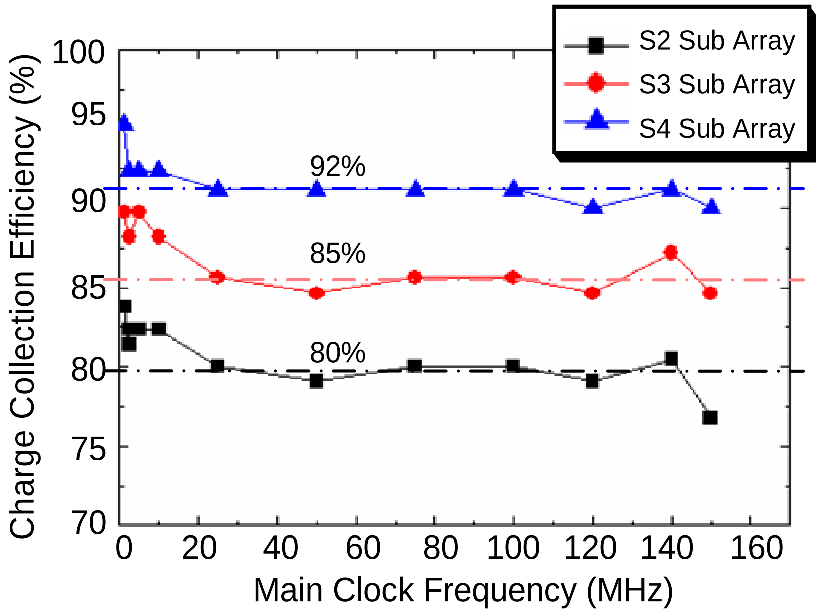
⇨ Noise

- Temporal noise independent of frequency up to 150 MHz (below 0.9 mV)
- Fixed pattern noise below 500 µV up to 100 MHz

⇨ Calibration peak

Peak's position independent of frequency

⇨ Charge collection efficiency (CCE) : defined as the ratio between the position of the charge collection peak and the position of the calibration peak.



The CCE is very weakly dependent on clocking frequency up to 125 MHz.
The lower the conversion factor (the larger the collecting diode) , the higher the CCE.

Summary of pre-irradiation characteristics

- Pixel level CDS → OK
- Fast readout : ~20μs per frame for the analog and digital outputs obtained in lab-tests
- Chip characteristics:

Sub Matrix	CVF (μV/e-)	Output Noise (mVrms)	Input Referred Noise (ENC)	S/N	FPN (mVrms)	Charge Collection Efficiency
S2	66	0.9	11 e-	130	≤ 0.5mV	80%
S3	60		12 e-	110		85%
S4	52		14 e-	90		92%

Neutron irradiation: physical aspects

- Simple calculations show that for an integrated flux of 10^{13} neutrons/cm^2 the total number of atomic collisions is of the order of 10^8 collisions /cm^2, assuming a 10 µm epitaxial layer thickness.
- Therefore for a 25 µm large pixel the number of primary collisions in the epi-layer is roughly 5
- For MeV energetic neutrons each primary collision induces a cascade of approximately 500 secondary displacements: the threshold energy for atomic displacements in silicon is 20 eV and the energy of the Primary Knock on Atom (PKA) is roughly 36 keV on average leading to around 500 secondary displacements
- The spatial extension of the defects (1 µm in average) results in clusters non-homogeneously distributed in the pixel

Neutron irradiation: experimental procedure

- Integrated fluxes from 10^{11} up to 10^{13} neutrons/cm^2
- Fast neutron irradiations made at CERI (Orléans), deuterons on a Be target
- After irradiation, functionalities of the readout on all chip remains OK
- Preliminary results of analog outputs are presented here for a low clocking frequency (1MHz)

Fast neutron spectrum

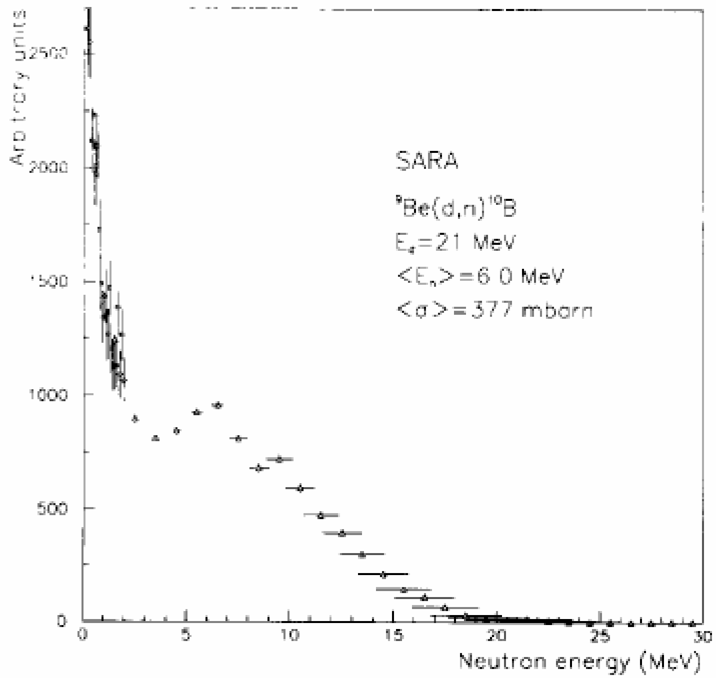


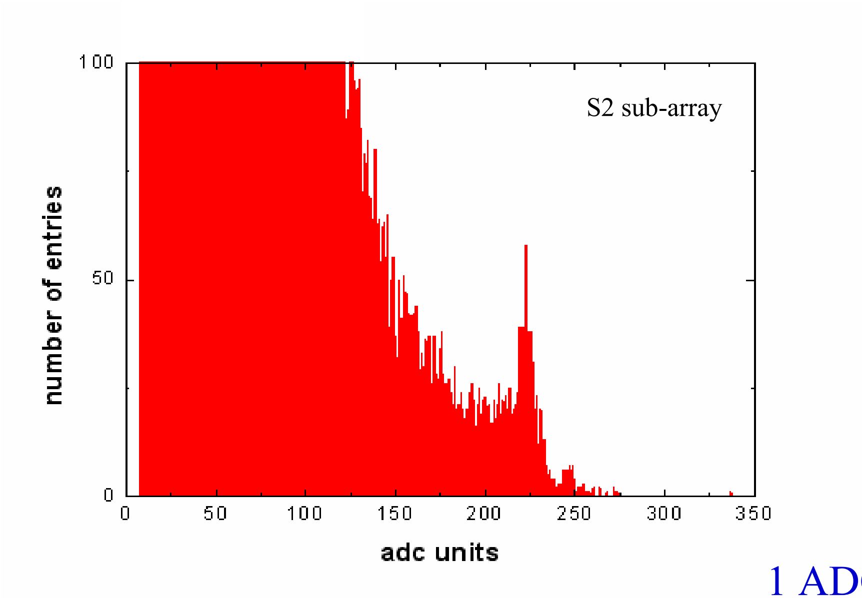
Fig. 4. Neutron energy spectrum measured at 0° with a threshold of 100 keV.

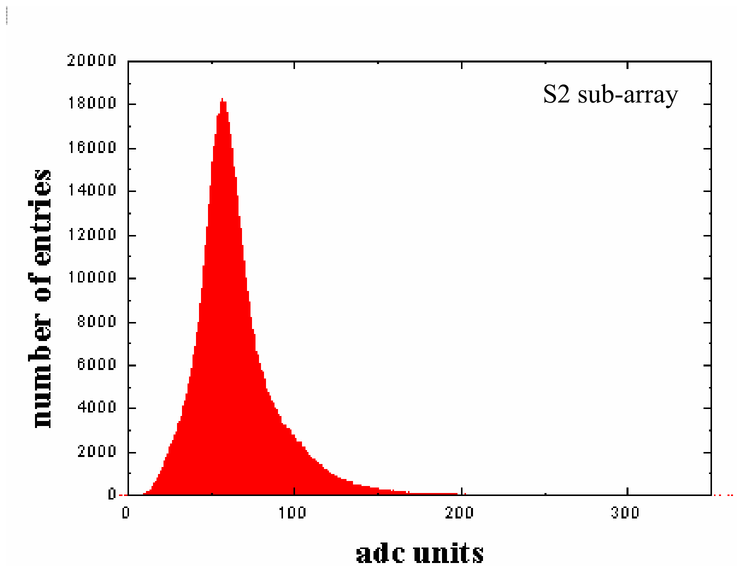
- Neutron flux as a function of energy for the source used

(reprinted from J. Collot et al., NIM A, vol.350, 525-529 (1994))

Spectra (most irradiated)

- >10^{13} neutrons/cm^2



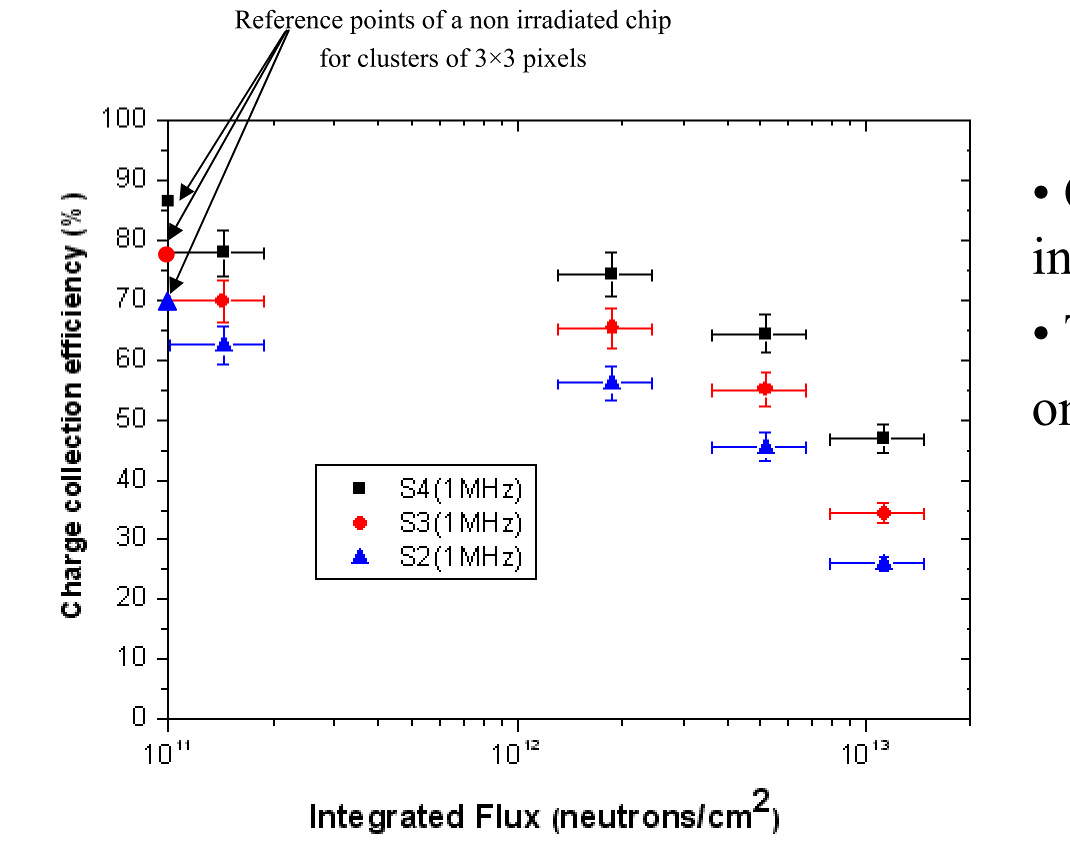


1 ADCU =0.5 mV

- Calibration peak
- 9 pixels clusters spectra

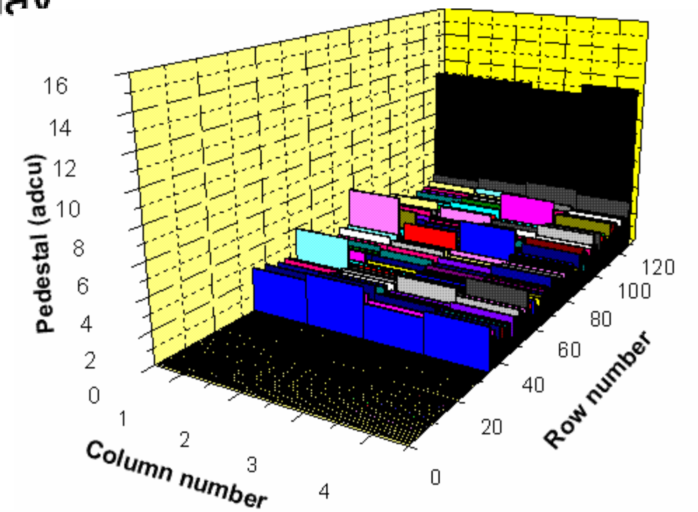
Charge collection efficiency(%)

at low frequency (1 MHz)



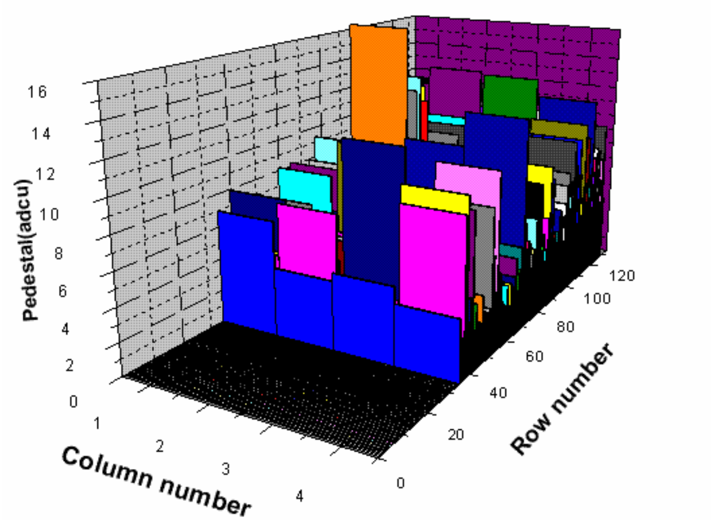
- Charge Collection Efficiency (CCE) in log scales.
- The points at the origin were obtained on a non-irradiated chip.

Pedestals (offsets)
at low frequency (1 MHz)



•3-D distribution of average pedestals for the S2, S3, S4 sub-arrays. The 4 columns and 128 rows were taken for a chip irradiated at 10^{11}n.cm^{-2}.

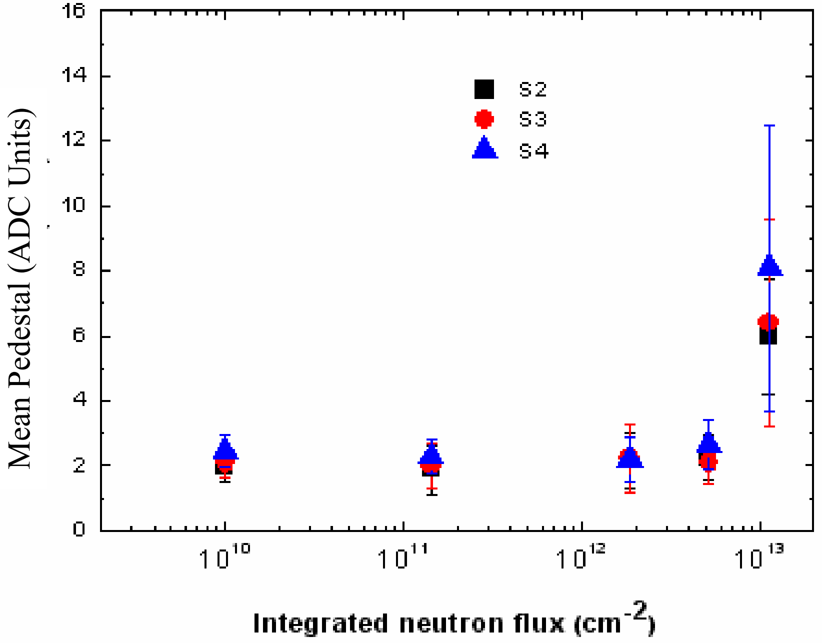
The pedestals corresponding to the S1 sub-array are not displayed.



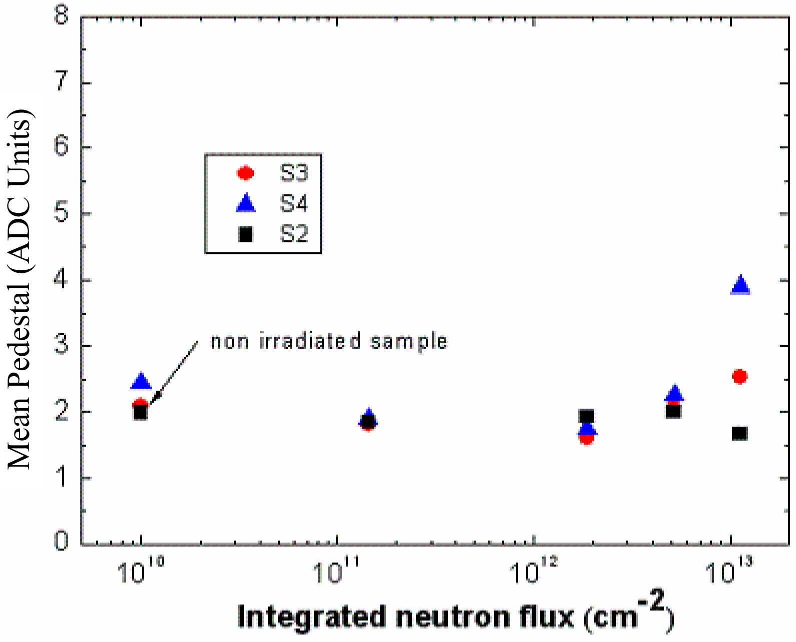
•Same 3-D distribution of pedestal for all sub-arrays for a chip irradiated at 1.1×10^{13}n.cm^{-2}.
The average pedestals values are randomly distributed.

Pedestals (offsets)
at low clocking frequency (1 MHz)

4 central columns



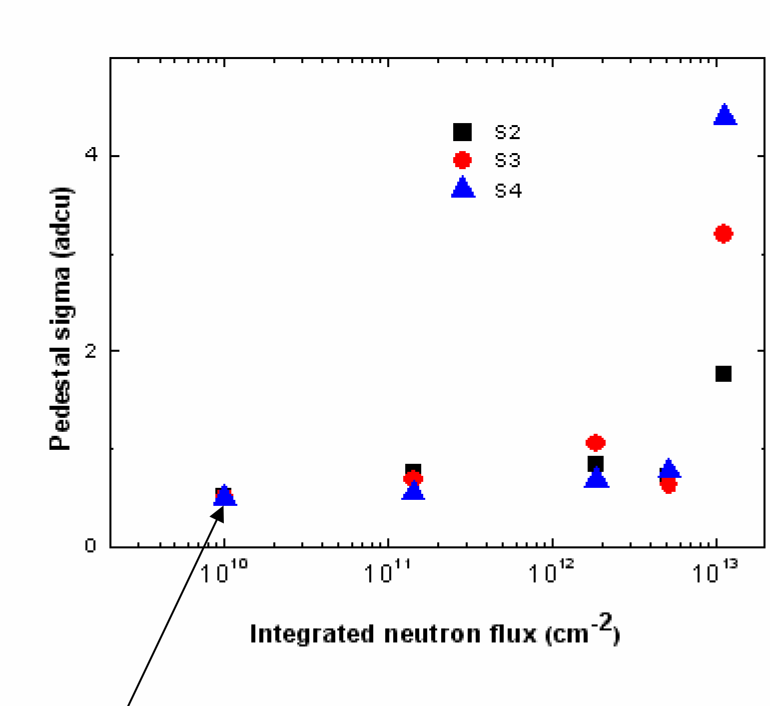
4 lateral columns



•Mean pedestals versus integrated neutron flux for the 8 analog columns

Fixed pattern noise

at low frequency (1 MHz)

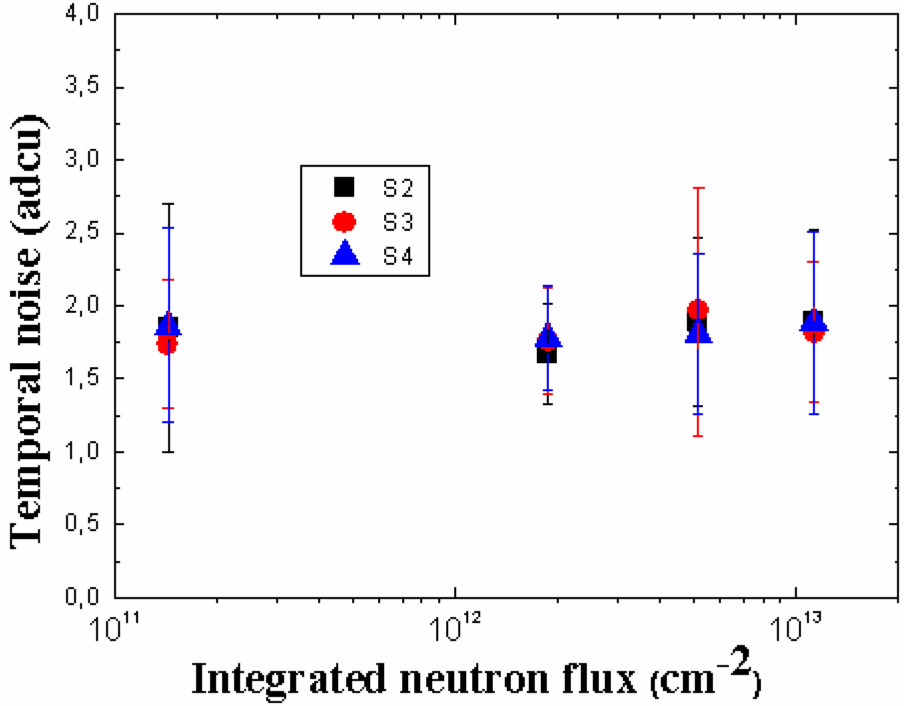


Reference points of a non irradiated chip

- Dispersion of the pedestals (Fixed Pattern Noise) plotted versus integrated neutron flux.
- The FPN only varies for fluxes above 10^{13} n/cm^2
- 10^{10} n/cm^2 points corresponds to the non-irradiation chip

dapnia cea saclay

Temporal noise
at low frequency (1 MHz)



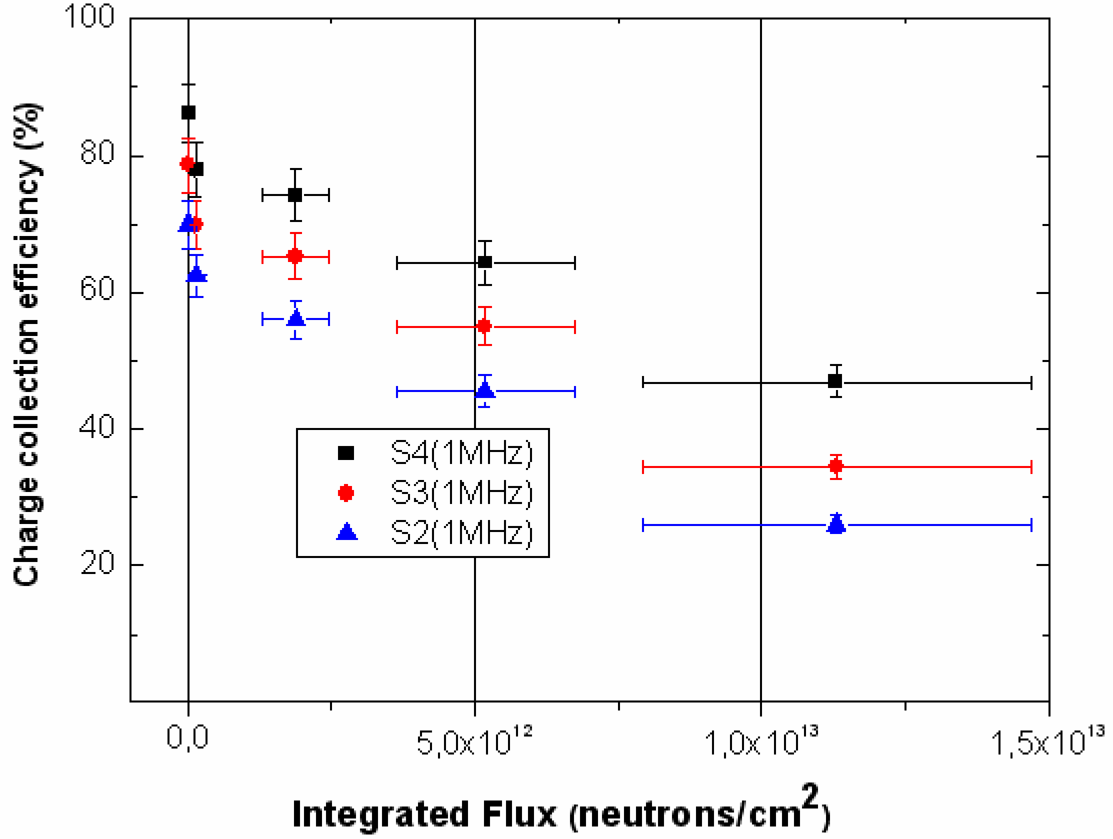
- The temporal noise remains unchanged with the integrated flux for all sub-arrays

Conclusions & Prospects

- Good overall characteristics up to 5.10^{12} n/cm^2
- Displacement damage has no significant effect on the circuitry

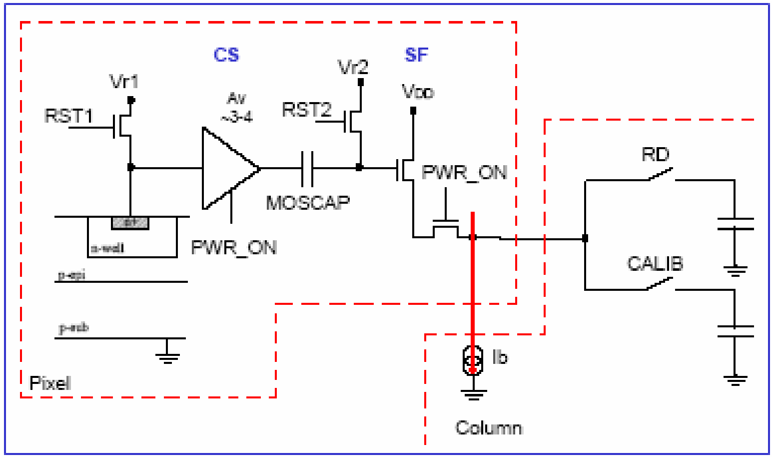
- More tests have to be done:
  - ionizing irradiation effects ^{60}Co
  - tests of neutrons effects at higher clocking frequencies
  - spatial resolution (September 2006)
  - device simulation to study scaling effects

- Submission of same architecture with 0.35µm AMS-Opto (MIMOSA16/HiMAPS-2)
- Implementation of an ADC (4-5 bits) for the digital output

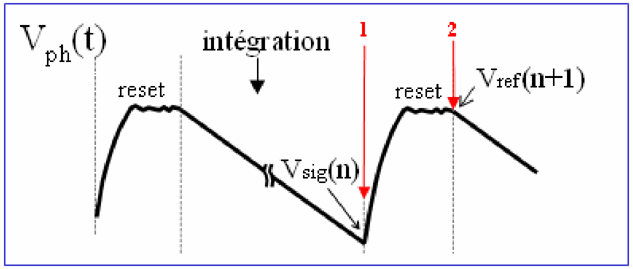

100
80
60
40
20
Charge collection efficiency (%)
0,0
5,0x10^12
1,0x10^13
1,5x10^13
Integrated Flux (neutrons/cm^2)
S4(1MHz)
S3(1MHz)
S2(1MHz)

The MIMOSA8/HiMAPS-1 chip

Principle of Correlated Double Sampling (CDS)



Photodiode :



✓1 : Vref + noise

✓2 : Vsig + noise

True signal = 2-1

In pixel CDS allows : pixel fixed pattern noise and reset noise suppression (no column FPN suppression)

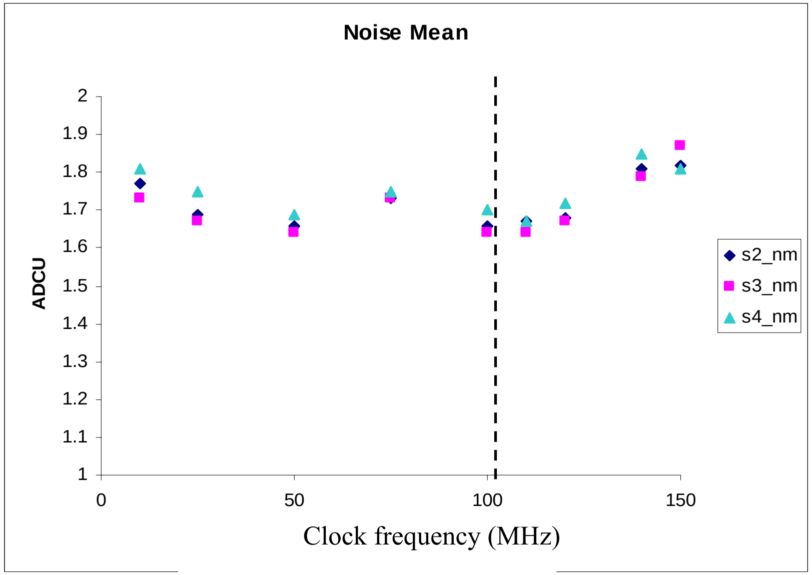
Analog outputs characterization

Two contributions to the total noise:

1) temporal noise ~ 0.9 mV (stable with frequency)
2) fixed pattern noise (pedestal dispersion) : ~ 0.5mV (stable up to 100 MHz)

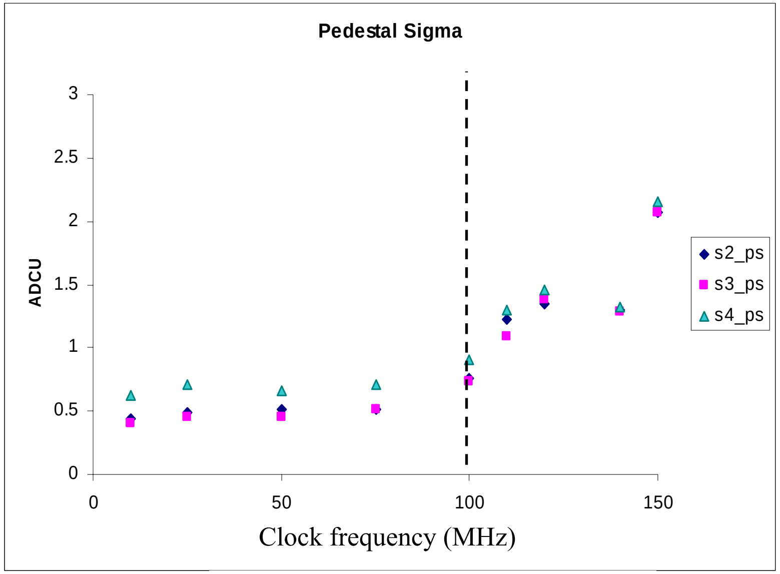
The design had been validated for a 100 MHz clock frequency:

The noise increases with frequency above 100 MHz as shown below



Temporal noise

(1 ADCU = 0.5mV)



Fixed pattern noise