Recent Development on CMOS Monolithic Active Pixel Sensors

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Outline

• Introduction: Vertex Detectors in future high energy physics experiments
• CMOS MAPS Solution
  - Principle of operation
  - Basic Read-Out Architecture
  - Typical performance
• Main R&D directions
• New MAPS in triple well with signal processing at the pixel level
• MAPS in future experiments
• Conclusions
Introduction

• Future high energy experiments (ILC, SuperBfactory...) will need an ultra-light (< 50 µm Si), very granular (~ 20 µm pitch), multi-layer vertex detector close to the interaction point, running in high occupancy and high radiation environments
  - The technology needs to combine high granularity, little multiple scattering, high read-out speed and radiation hardness
• Existing pixel detector technology not adequate:
  - CCD: too slow and radiation soft
  - Hybrid Pixel Sensors: not granular and thin enough

• **CMOS Monolithic Active Pixel Sensors (MAPS)**, developed for visible light imaging in early ‘90s, look very promising for application in future tracking devices
**Principle of Operation**

- Signal generated by a particle is collected by a diode (n-well/p-epitaxial layer), then readout by CMOS electronics integrated in the same substrate... **BUT**:
  - Charge generated by the incident particle moves by thermal diffusion in the thin (~ 10 μm) p-epitaxial layer
    - P-epi layer doping ~10¹⁵ cm⁻³
      - not depleted
      - carrier lifetime O(10 μs), small diffusion distance
  - P++ substrate gives a small contribution to the collected charge (very low carrier lifetime)
  - Typical M.I.P. signal depends on epitaxial thickness (saturates for p-epi ~ 20 μm)
    - Q ~ 80 e-h/μm -> Signal ~ 1000 e-
  - Typical collection time: ≤ 100 ns for small diode, faster with larger diodes.
  - Charge-to-voltage conversion provided by sensor capacitance -> small collecting electrode
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Advantages of CMOS MAPS

- Same substrate for detector & readout:
  - System-on-chip, compact and flexible
- **MAPS** sensitive volume only 10-15 µm thick
  - thin down to < 50 µm possible
  - less material in the detection region w.r.t hybrid pixel
- Sensor faster and more rad hard than **CCDs**
  - no charge transport along the sensor volume
- **CMOS** commercial process
  - low power consumption and fabrication costs
  - high functional density and versatility
  - electronics intrinsically radiation hard (deep submicron tech.)
Basic (3T) readout principle

- Pixel reset periodically: to compensate diode leakage current and remove collected charge from previous event
- Pixel selected & sampled twice during integration time: $t_{fr2} - t_{fr1}$ = time to readout the entire frame.
- Sequential readout of all pixels in the frame

- Offline signal extracted subtracting data from two consecutive samplings, before-after particle arrival (CDS) and removing pedestal from leakage current

Only 3 Transistors inside pixel cell: reset, select & sense

Pixel Voltage vs. time

- $\Delta V_{typ} \alpha I_{leak}$
- $\Delta V_{sig} \alpha Q_{signal}$

Integration time

Integration time $t_{fr2} - t_{fr1}$

Pixel Array: Column select – ganged row read

Array of pixels

High-speed

ADC

& storage
Correlated Double Sampling (CDS)

Frame 1 - Frame 2 = 

- Leakage current Correction

~fA leakage current (typ) 
~18fA for hottest pixel shown

Hit candidate!

G. Varner (Hawaii), CAP sensors

8ms integration shown

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MAPS activities around the world

- With first MAPS prototypes (basic 3T architecture and sequential readout) low noise detection of M.I.P demonstrated in 2001

- Since then the MAPS community has grown and is very active
- Non exhaustive list:
  - MIMOSA series (Strasbourg, Saclay, Clermont, Grenoble)
    - Minimum Ionizing MOS Active sensor
  - FAPS series (RAL, Liverpool)
    - Flexible Active Pixel Sensor
  - CAP series (Univ. Hawaii)
    - Continuous Acquisition Pixel
  - BNL,LBL,Univ.Oregon&Yale
  - Univ.Pisa/Pavia/Bergamo/Trieste/Bo (SLIM5-Collaboration)
  - Univ.Perugia/Parma (RAPS)
  - Others...
Main R&D Directions

• Results in first 6 years of R&D very encouraging:
  – Excellent M.I.P. detection efficiency and single point resolution established for several prototypes.

- Optimal fabrication process vs. epitaxial layer thickness, # metal layers, yield, dark current, cost, lifetime of process:
  – Many technologies explored:
    • AMS-0.6µm (14 µm), 0.35µm (0 !!!), 0.35µm OPTO (10-11 µm),
    • AMI (former MIETEC)-0.35µm (4 µm), IBM-0.25µm (2 µm),
    • TSMC-0.35µm (~10-12 µm ?), TSMC-0.25µm (≤8 µm), STM-0.13 µm,  Others ???

- Radiation Tolerance investigated partly: good performance obtained

- Industrial thinning procedure
  - satisfactory outcome from first prototype (50 µm)
  - Minimal thickness, individual chips rather than wafer, yield ??

• Fast integrated signal processing concentrates the efforts:
  • High readout speed, low noise, low power, highly integrated signal processing architectures needed to meet detector requirements
    • ILC :

<table>
<thead>
<tr>
<th>Layer</th>
<th>Pitch</th>
<th>t_r.o.</th>
<th>N_{lad}</th>
<th>N_{pix}</th>
<th>P_{inst}^{diss}</th>
<th>P_{mean}^{dis}</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO</td>
<td>20 µm</td>
<td>25 µs</td>
<td>20</td>
<td>25M</td>
<td>&lt; 100 W</td>
<td>&lt; 5 W</td>
</tr>
</tbody>
</table>

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Overview of Achieved Performances

- Several MIMOSA prototypes (Strasbourg et al.) tested with H.E. beam (SPS, DESY) → well established performance:
  - \( N \sim 10 \text{ e}^-, \ S/N \sim 20-30 \) (MPV) \( \Rightarrow \varepsilon_{\text{det}} \sim 99.5\% \), \( \sigma_{\text{sp}} = 1.5-2.5 \ \mu\text{m} \) (20 \( \mu\text{m} \) pitch)
  - Best performing technology: AMS-0.35\( \mu\text{m} \) OPTO (12 \( \mu\text{m} \) epi layer)
  - Technology without epitaxial layer performs well (high S/N) but gives larger clusters (poor hit separation)
  - Macroscopic sensors: MIMOSA V(1.9x1.7\( \text{cm}^2 \); 1Mpix), CAP-3(0.3x2.1\( \text{cm}^2 \); 120kpix)

**M9: S/ N in seed pixel**

MPV \~ 26

**M9: Efficiency vs Temp.**

**Sp. resol. vs pitch**

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Radiation Tolerance

- **Transistors** - In modern deep submicron tech. (eventually with special layout rules) they may be rad hard up to tens of Mrads and up to fluences of $10^{15}$ p/cm$^2$

- **Diodes** - Radiation damage affects S/N.
  - Non-ionizing radiation: bulk damage cause charge collection reduction, due to lower minority carrier lifetime (trapping)
    - fluences $\sim 10^{12}$ n$_{eq}$/cm$^2$ affordable, $10^{13}$ n$_{eq}$/cm$^2$ possible
  - Ionizing radiation:
    - noise increase, due to higher diode leakage current (surface damage)
      - OK up to 20 Mrad with low integration time (10 $\mu$s) or
        - $T$ operation $< 0^\circ C$, or modified pixel design to improve it
    - charge loss also observed, technology dependent, probably related to positive charge build-up in thick oxide (under study)
Non-Ionizing Radiation

- Irradiation with neutron/proton with fluences up to $10^{13-14}$ p/cm$^2$
  - Charge loss at $10^{12}$ n$_{eq}$/cm$^2$
  - Modest increase of leakage and noise $\sim 10\%$

- S/N (MPV) vs fluence and $T$
- Fluence of $\geq 10^{12}$ n$_{eq}$/cm$^2$ affordable ($T \leq 0^\circ C$) Effi det $\sim 99.7\%$

<table>
<thead>
<tr>
<th>Fluence</th>
<th>$T = -20^\circ C$</th>
<th>$T = 0^\circ C$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$28.4 \pm 0.2$</td>
<td>$26.3 \pm 0.2$</td>
</tr>
<tr>
<td>$10^{11}$ n$_{eq}$/cm$^2$</td>
<td>$25.3 \pm 0.2$</td>
<td>$24.5 \pm 0.4$</td>
</tr>
<tr>
<td>$3 \cdot 10^{11}$ n$_{eq}$/cm$^2$</td>
<td>—</td>
<td>$23.0 \pm 0.2$</td>
</tr>
<tr>
<td>$10^{12}$ n$_{eq}$/cm$^2$</td>
<td>$18.7 \pm 0.2$</td>
<td>—</td>
</tr>
</tbody>
</table>

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Ionizing Radiation Effects

• Leakage current saturates @ 5Mrad after proper annealing.
• Noise from leakage increases:

\[ V_n^2(t_{int}) = \frac{qI_{leak}^2}{C^2} t_{int} \]
• S/N reduction still modest for short integration time (<100 µs)

• Aim for short integration time and low Toperation
  OR
  modify pixel design to keep leakage current increase under control (next slide)

CAP (Hawaii) Prototypes irradiated with \(\gamma\) (\(^{60}\text{Co}\)) up to 20 Mrad

S/N vs dose


Belle CAP1 Prototype

Fully annealed

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Reduce Ionizing Radiation Effects

Modified pixel design
→ avoid thick oxide near the N-well

Leakage contribution for irradiated sensor is dominated by surface defects at the interface between thick oxide and silicon

10 keV X-ray

Beamtest on MIMOSA11

Running conditions: +40°C, 700 μs readout time

New

After 20 kRad

Standard pixel (A0 Sub 2)
S/N (MPV): 23.9 | 10.3
Det Eff [%]: 99.9 | 97.7
Noise [e-]: 10.7 | 23.5

Hardened pixel (A0 Sub 1)
S/N (MPV): 14.9 | 15.1
Det Eff [%]: 99.5 | 99.6
Noise [e-]: 16.1 | 16.1

Still room for improvement

• Noise vs. integration time and Toperation confirmed modified design is effective
• Hardened pixel OK @ 1 Mrad at T < 0°C

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Thinning

- **MIMOSA-5 wafers**: 120 µm sensor thickness repeatedly achieved
  - ⇒ no performance loss observed (several chips tested)

- **MIMOSA-5 chips thinned to 50 µm**
  - via LBNL for STAR VD upgrade
    ⇒ Very Preliminary results
      @ room Temperature (1.5 GeV e-)
  - TRACIT company (Europe):
    • successful (mech.)
    ⇒ electrical tests foreseen

On going tests to thin down chips to 35-40 µm

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High Readout Speed MAPS

- First MAPS prototypes realized with the basic 3T architecture and sequential readout showed very good results with M.I.P. but:
  - Extremely simple in-pixel readout configuration (3T)
  - sequential readout → limitation for large detector: ~1 kHz sampling rate for Megapixel array

- Two main R&D directions to improve the readout speed with basic 3T readout:
  - Pipeline design: charge sampled and stored inside pixel at high rate (100 KHz-10 MHz) readout delayed at slower rate (only interesting time window readout, or data transferred during no beam time window) → FAPS, CAP, MIMOSA 12
  - Parallel digital processing: signal processing at the column level → MIMOSA 8

- Different approach: MAPS with full signal processing at the pixel level (hybrid-pixel-like), designed exploiting triple well option available in CMOS commercial process. Readout easily compatible with data sparsification → high readout speed potential (SLIM5 Collaboration)
Flexible Active Pixel Sensor (FAPS, RAL): TSMC 0.25/8, 10 memory cell/pixel; 28 transistor/pixel; 3 sub-arrays of 40x40 pixels @20 um pitch; sampling rate up to 10 MHz; Noise ~ 40 e- rms, single-ended readout. S/N=15-17.

Continuous Acquisition Pixel (CAP, Hawaii): 3 versions produced in TSMC 0.35/8 and 0.25/8, 5 pairs cell/pixel in CAP3; Noise 40-50 e- rms single ended →20-25 e- differential. Sampling rate 100 KHz with CAP2.

MIMOSA 12 (Strasbourg et al.) in AMS 035/14: 4 pairs cell/pixel (35 um pitch), exploring various dimensions of memory cell.
Parallel read-out architecture: MIMOSA 8

- **Test beam results** (DESY, 5GeV e-)
  - Analog part
    - Typical noise $\Rightarrow \sim 12$-$15$ e-
    - $S/N$ (MPV) $\sim 9$ $\Rightarrow$ thin epi layer
    - Pixel-to-pixel dispersion $\sim 8$ e-
  - Digital part: the discriminator works as expected:
    - TSMC 0.25 $\mu$m fab. process with $\sim 8$ $\mu$m epi layer
    - Pixel pitch: 25 $\mu$m
    - CDS on pixel with 2 memory cell
    - 24 parallel columns (128 pixels) with 1 discriminator per column
    - 8 analogic columns

- **Hit Efficiency (%) vs S/N cut**
- **Fake hit rate (%) vs S/N cut**

- Excellent detection performance despite modest epi layer thickness
- Architecture validated for next steps: tech. with thick epi layer, rad. Tolerant pixel at Troom, ADC, sparsification etc.
Triple well CMOS MAPS (I)

- Use of commercial triple-well CMOS process proposed to address some limitations of conventional MAPS
  - improve readout speed with in-pixel signal processing
  - improve single pixel signal with a larger collecting electrode

In triple-well processes a deep n-well is used to provide N-channel MOSFETs with better insulation from digital signals

This feature exploited for a new approach in the design of CMOS pixels:
- The deep n-well can be used as the collecting electrode
- A full signal processing circuit can be implemented at the pixel level overlaying NMOS transistors on the collecting electrode area
Triple well CMOS MAPS (II)

- Standard processing chain for capacitive detector implemented at pixel level

  - Charge preamplifier used for Q-V conversion:
    - Gain is independent of the sensor capacitance -> collecting electrode can be extended to increase the signal
  - RC-CR shaper with programmable peaking time (0.5, 1 and 2 \(\mu s\))
  - A threshold discriminator is used to drive a NOR latch featuring an external reset

- Fill factor = deep n-well/total n-well area \(\geq 0.85\) in the prototype test structures \(\rightarrow\) high detection efficiency

- Readout scheme compatible with existent architectures for data sparsification at the pixel level \(\rightarrow\) improve readout speed

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Triple Well MAPS Results

- First prototype chip, with single pixels, realized in 0.13 \( \mu \text{m} \) triple well CMOS process (STMicroelectronics)
- Very encouraging results:
  - Proof of principle
  - \( S/N = 10 \) \(^{90}\text{Sr} \) \( \beta \) source
    - Single pixel signal ~1250e-
      (only 300 e- in conventional MAPS!)
    - High pixel noise ENC = 125 e-
      (due to underestimated deep nwell capacitance)
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    (due to underestimated deep nwell capacitance)

Second prototype under test:

- Pixel matrix (8x8, 50x50 \( \mu \text{m}^2 \)) with simple sequential readout tested up to 30 MHz.
- Pixels with varying electrode size (900-2000 \( \mu \text{m}^2 \))
- Improved front-end: pixel noise ENC = 50 e-
  \( \rightarrow \) M.I.P. Expected \( S/N \) ~ 25
- Problems: threshold dispersion measured ~300 e-, ground line bouncing in digital transitions.
Next steps for triple well MAPS

- Final ambitious goal of the SLIM5 Collaboration is to design a monolithic pixel sensor with similar readout functionalities as in hybrid pixels (sparsification, time stamping), suitable to be used in a trigger (L1) system based on associative memories.
  - Test beam in 2008.
- First triple well MAPS prototypes (0.13 µm-ST), with full signal processing at the pixel level, demonstrated capability to detect ionizing radiation with good S/N.
- Next prototypes (Aug-Nov '06) will improve significantly threshold dispersion (to noise level) and test readout architecture with data sparsification and time stamp.
- Radiation Tolerance should still be investigated:
  - Design with large collecting electrode expected to be more rad hard against non-ionizing radiation.
  - Charge preamp. with continuous reset less sensitive to leakage current increase from ionizing radiation
Applications of MAPS in future experiments

- First detectors made of CMOS MAPS coming soon:
  - MIMOSA sensors will equip
  - STAR Heavy Flavour Tagger:
    - 2008 analog output, 4 ms readout time
    - 2011 digital output ~ 200 µs frame r.o. time
  - EUDET beam telescope for ILC R&D:
    - 2007 demonstrator with analog output
    - 2008 final device with digital output

- CMOS MAPS developed also for:
  - ILC Vertex Detector: R&D France, UK, USA, Italy...
  - SuperBFactory Vertex Detector: R&D in Hawaii (Belle), Italy (BaBar)
Conclusions

• Future vertex detectors need a new technology (granular, thin, fast…) and CMOS sensors could potentially accommodate all the requests
• Excellent tracking performance established in the first years of R&D on CMOS MAPS
• The MAPS community, very active and still growing, has still a lot to do in the coming years to convert a good idea into a real operating detector for the most challenging applications
• Main R&D directions:
  - High readout speed MAPS, digital output & sparsification
  - Radiation tolerance
  - Thinning procedure
  - New fabrication processes