Recent Development on CMOS Monolithic Active Pixel Sensors

Tracking detector applications

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8th International Workshop on Radiation Imaging Detectors
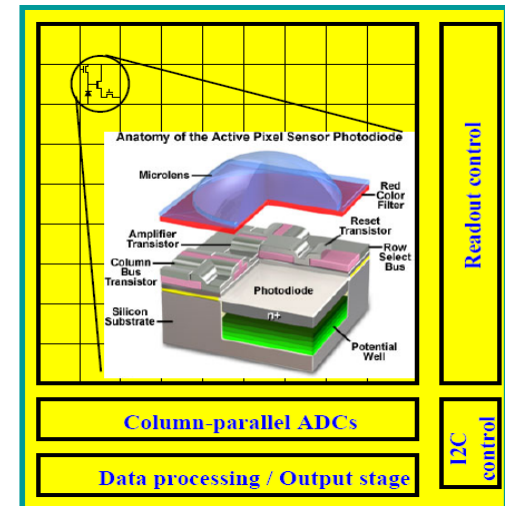
Pisa, July 2-6 2006

Outline

- Introduction: Vertex Detectors in future high energy physics experiments
- CMOS MAPS Solution
  - Principle of operation
  - Basic Read-Out Architecture
  - Typical performance
- Main R&D directions
- New MAPS in triple well with signal processing at the pixel level
- MAPS in future experiments
- Conclusions

Introduction

- Future high energy experiments (ILC, SuperBfactory…) will need an ultra-light (< 50 μm Si), very granular (~ 20 μm pitch), multi-layer vertex detector close to the interaction point, running in high occupancy and high radiation environments
  - The technology needs to combine high granularity, little multiple scattering, high read-out speed and radiation hardness
- Existing pixel detector technology not adequate:
  - CCD: too slow and radiation soft
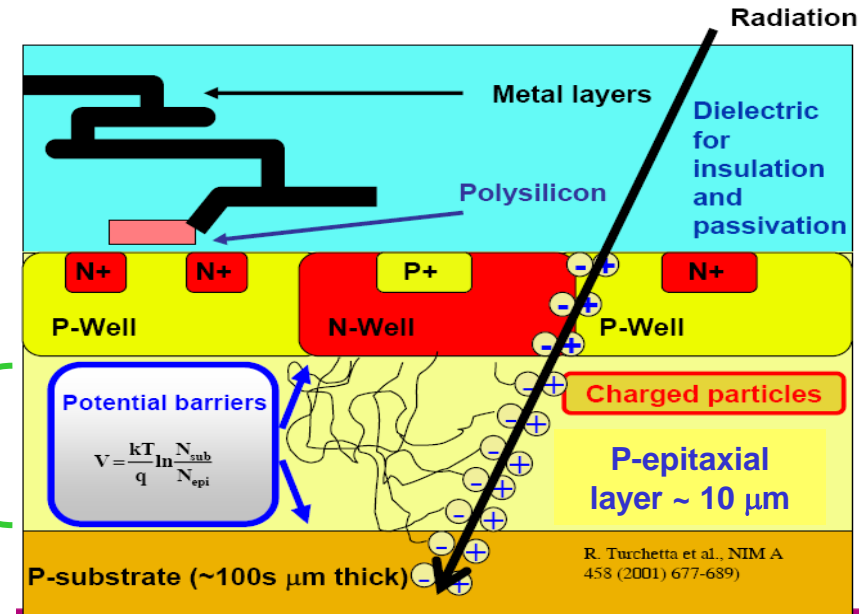 - Hybrid Pixel Sensors: not granular and thin enough

- CMOS Monolithic Active Pixel Sensors (MAPS), developed for visible light imaging in early '90s, look very promising for application in future tracking devices

Anatomy of the Active Pixel Sensor Photodiode

Microlens — Red Color Filter

Amplifier Transistor — Reset Transistor

Column Bus Transistor — Row Select Bus

Silicon Substrate — Photodiode — n+

Potential Well

Readout control

Column-parallel ADCs

I2C control

Data processing / Output stage

Principle of Operation

- Signal generated by a particle is collected by a diode (n-well/p-epitaxial layer), then readout by CMOS electronics integrated in the same substrate... **BUT** :
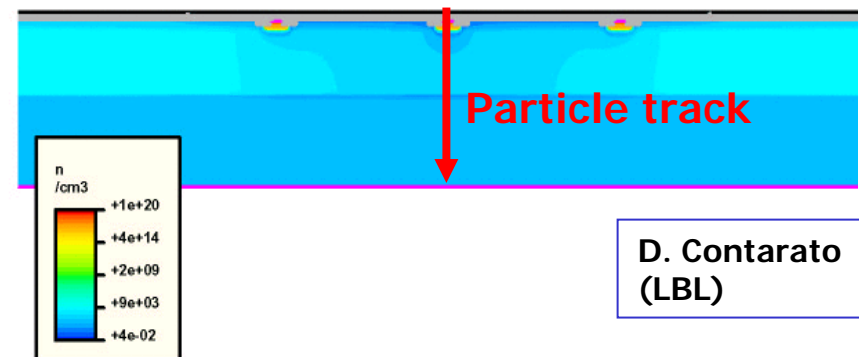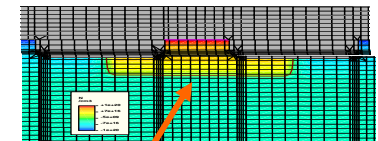
- Charge generated by the incident particle moves by thermal diffusion in the <u>thin (~ 10 μm) p-epitaxial layer</u>
  - P-epi layer doping ~10^{15} cm^{-3}
  - → not depleted
  - → carrier lifetime O(10 μs), small diffusion distance
- P++ substrate gives a small contribution to the collected charge (very low carrier lifetime)
- Typical M.I.P. signal depends on epitaxial thickness (saturates for p-epi ~ 20 μm)
  - **Q ~ 80 e-h/μm -> Signal ~ 1000 e-**
- Typical collection time: ≤ 100 ns for small diode, faster with larger diodes.
- Charge-to-voltage conversion provided by sensor capacitance -> small collecting electrode

Radiation
Metal layers
Dielectric for insulation and passivation
Polysilicon
N+ N+ P+ N+
P-Well N-Well P-Well
Potential barriers
$$V = \frac{kT}{q} \ln \frac{N_{sub}}{N_{epi}}$$
Charged particles
P-epitaxial layer ~ 10 μm
R. Turchetta et al., NIM A 458 (2001) 677-689)
P-substrate (~100s μm thick)

Device Simulation (ISE-TCAD)

Charge collection movie ~ 100 ns

Mimosa V
Pixel pitch 17 μm, diode 3 μm, EPI-thickness 14 μm

n /cm3
+1e+20
+4e+14
+2e+09
+9e+03
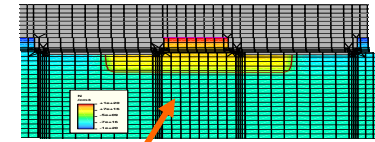+4e-02

Particle track

D. Contarato (LBL)

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Device Simulation (ISE-TCAD)

Charge collection movie ~ 100 ns

**Mimosa V**
Pixel pitch 17 μm, diode 3 μm, EPI-thickness 14 μm

Particle track

0 nsec

1 nsec

10 nsec
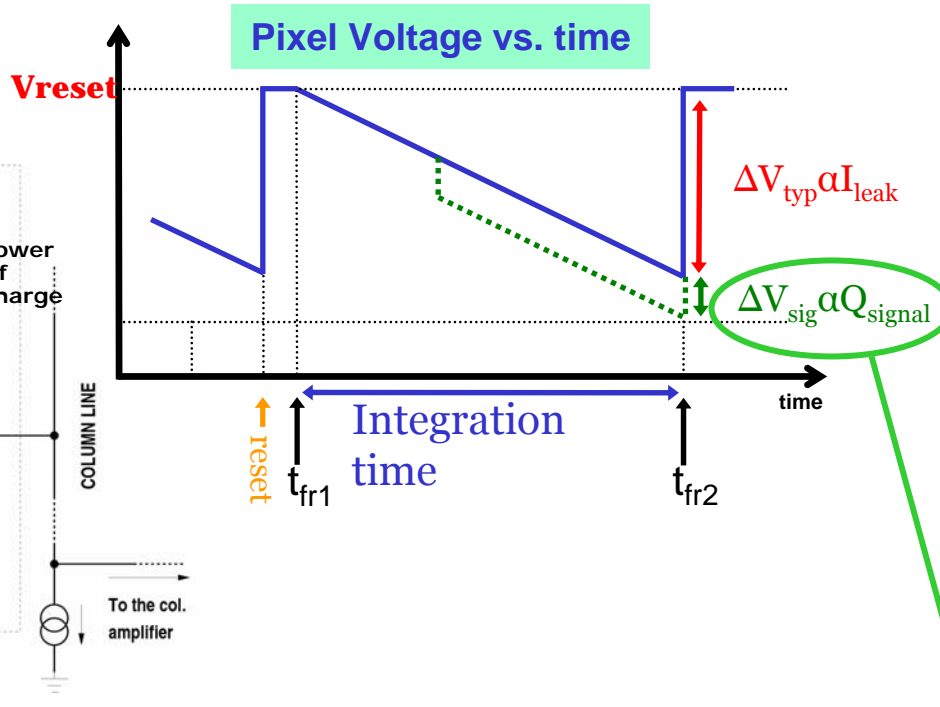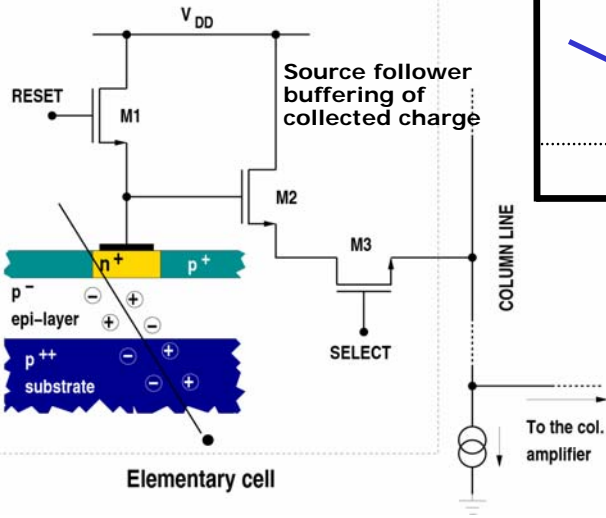
20 nsec
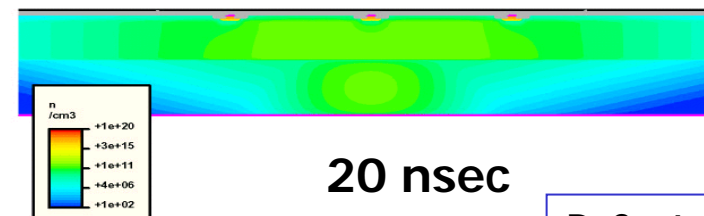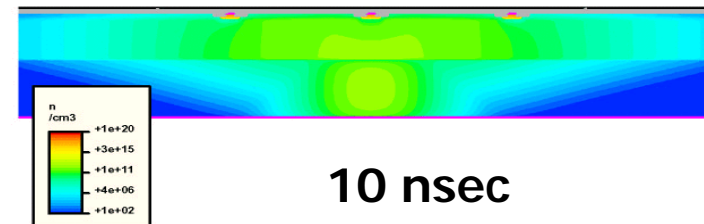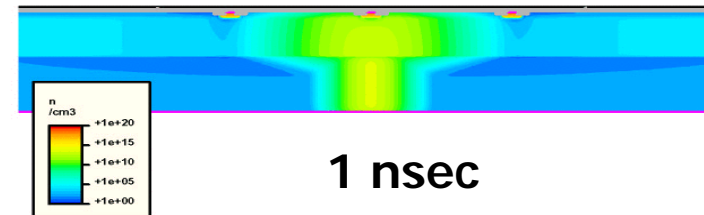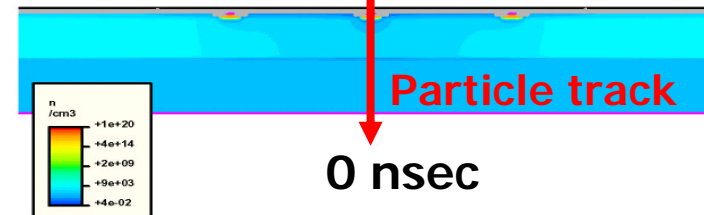
D. Contarato (LBL)

Advantages of CMOS MAPS

- Same substrate for detector & readout:
    - System-on-chip, compact and flexible
- MAPS sensitive volume only 10-15 μm thick
    - → thin down to < 50 μm possible
    - → less material in the detection region
      w.r.t hybrid pixel
- Sensor faster and more rad hard than CCDs
    - → no charge transport along the sensor volume

- CMOS commercial process
    - low power consumption and fabrication costs
    - high functional density and versatility
   - electronics intrinsically radiation hard
      (deep submicron tech.)

chip

front end electronics

bump connection

sensor

Hybrid pixel sensor

Direction of transfer
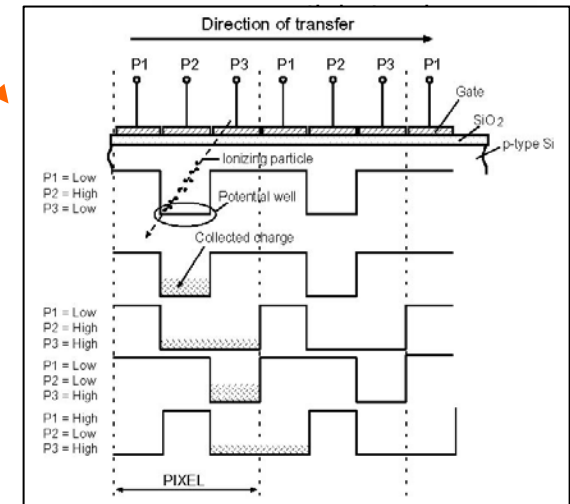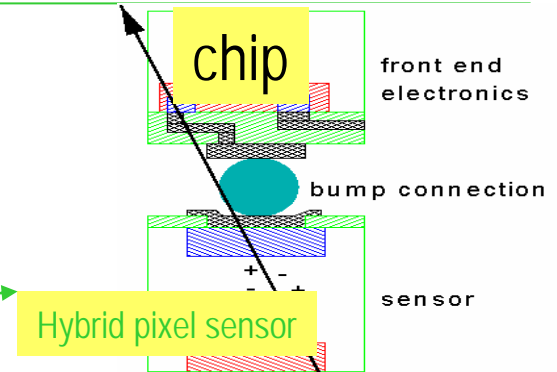
Basic (3T) readout principle

Only 3Transistors inside pixel cell: reset,select& sense

Source follower buffering of collected charge

V_{DD}

RESET — M1

M2

M3

n^+ p^+

p⁻ epi-layer

p⁺⁺ substrate

SELECT

COLUMN LINE

To the col. amplifier

Elementary cell

Pixel Voltage vs. time

Vreset

$\Delta V_{typ} \alpha I_{leak}$

$\Delta V_{sig} \alpha Q_{signal}$

reset t_{fr1}

Integration time

t_{fr2}

time

- Pixel reset periodically: to compensate diode leakage current and remove collected charge from previous event

- Pixel selected&sampled twice during integration time: $t_{fr2} - t_{fr1}$ =time to readout the entire frame.

- Sequential readout of all pixel in the frame

Pixel

Array of pixels
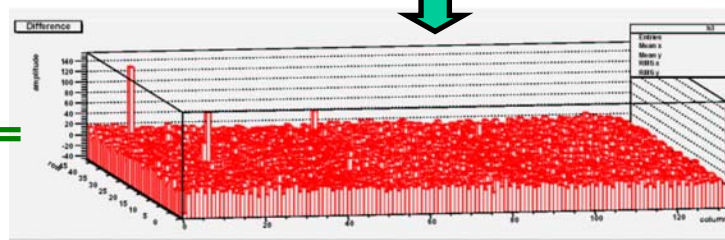
High-speed

analog

ADC

& storage
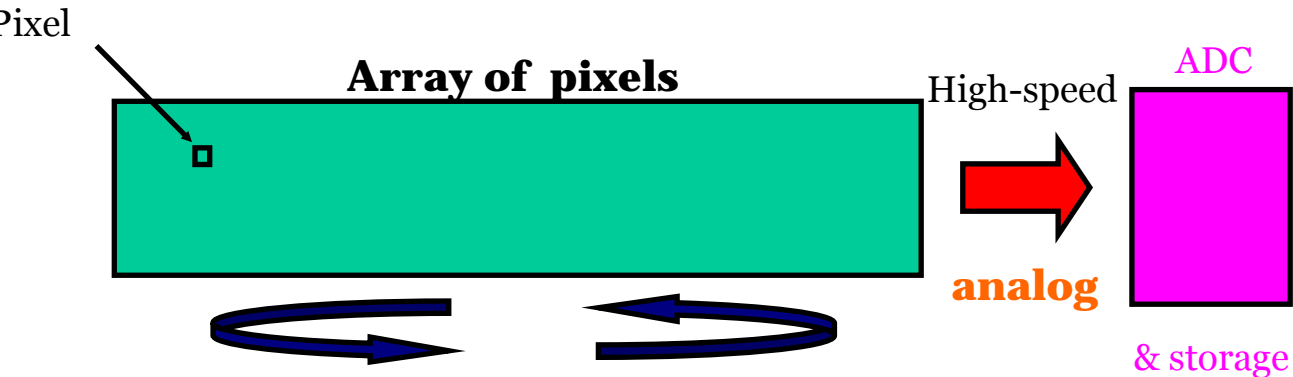
- Offline signal extracted subtracting data from two consecutive samplings, before-after particle arrival (CDS) and removing pedestal from leakage current

Pixel Array: Column select – ganged row read
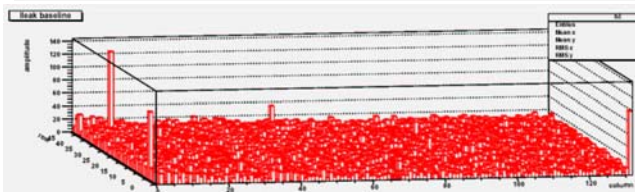
Correlated Double Sampling (CDS)
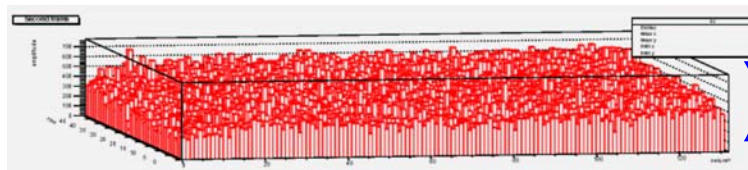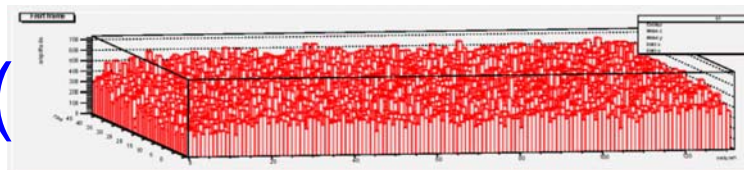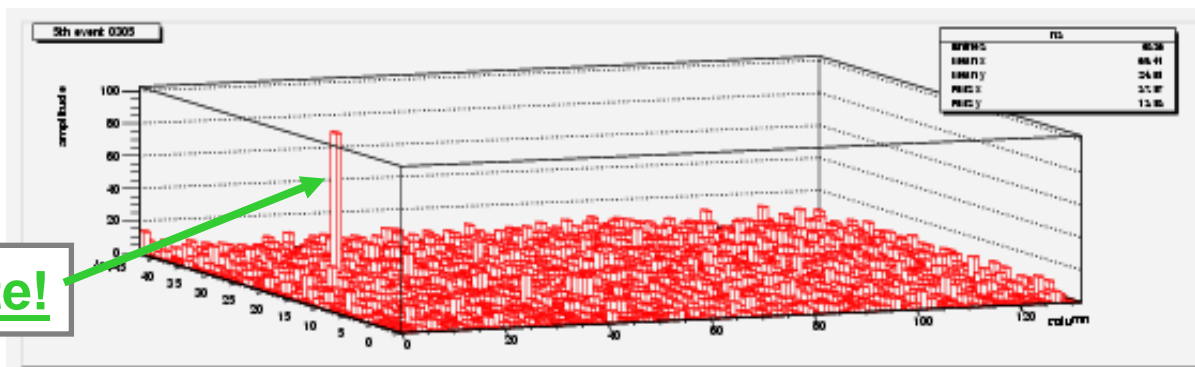

Frame 1 - Frame 2 =

- Leakage current Correction

~fA leakage current (typ)
~18fA for hottest pixel shown

8ms integration shown
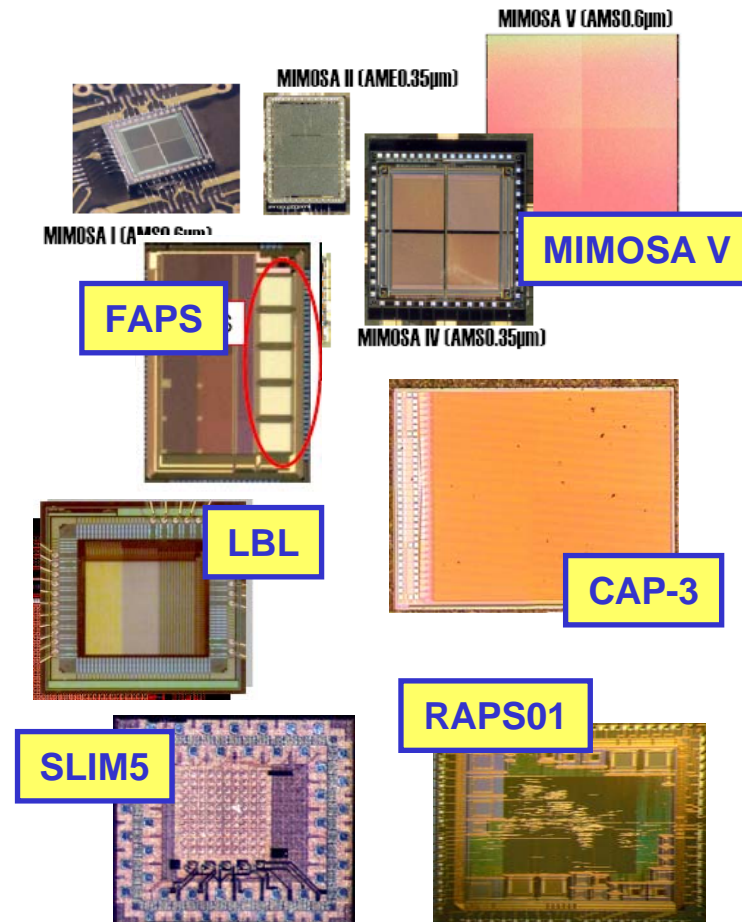
G. Varner (Hawaii), CAP sensors

Hit candidate!

MAPS activities around the world

- With first MAPS prototypes (basic 3T architecture and sequential readout) low noise detection of M.I.P demonstrated in 2001

- Since then the MAPS community has grown and is very active
- Non exhaustive list:
  - MIMOSA series (Strasbourg, Saclay, Clermont, Grenoble)
    - Minimum Ionizing MOS Active sensor
  - FAPS series (RAL, Liverpool)
    - Flexible Active Pixel Sensor
  - CAP series (Univ. Hawaii)
    - Continuous Acquisition Pixel
  - BNL,LBL,Univ.Oregon&Yale
  - Univ.Pisa/Pavia/Bergamo/Trieste/Bo (SLIM5-Collaboration)
  - Univ.Perugia/Parma (RAPS)
  - Others...

MIMOSA V (AMS0.6µm)

MIMOSA II (AME0.35µm)

MIMOSA I (AMS0.6µm)

MIMOSA IV (AMS0.35µm)

MIMOSA V

FAPS

LBL

CAP-3

RAPS01

SLIM5

Main R&D Directions

- **Results in first 6 years of R&D very encouraging:**
  - Excellent M.I.P. detection efficiency and single point resolution established for several prototypes.

- **Optimal fabrication process** vs. epitaxial layer thickness, # metal layers, yield, dark current, cost, lifetime of process:
  - Many technologies explored:
    - AMS-0.6μm (14 μm), 0.35μm (0 !!!), 0.35μm OPTO (10-11 μm),
    - AMI (former MIETEC)-0.35μm (4 μm), IBM-0.25μm (2 μm),
    - TSMC-0.35μm (~10-12 μm ?), TSMC-0.25μm ($\leq$8 μm), STM-0.13 μm,   Others ???
- **Radiation Tolerance** investigated partly: good performance obtained
- **Industrial thinning procedure**
  - satisfactory outcome from first prototype (50 μm)
  - Minimal thickness, individual chips rather than wafer, yield ??
- **Fast integrated signal processing concentrates the efforts:**
  - High readout speed, low noise, low power, highly integrated signal processing architectures needed to meet detector requirements
    - ILC :

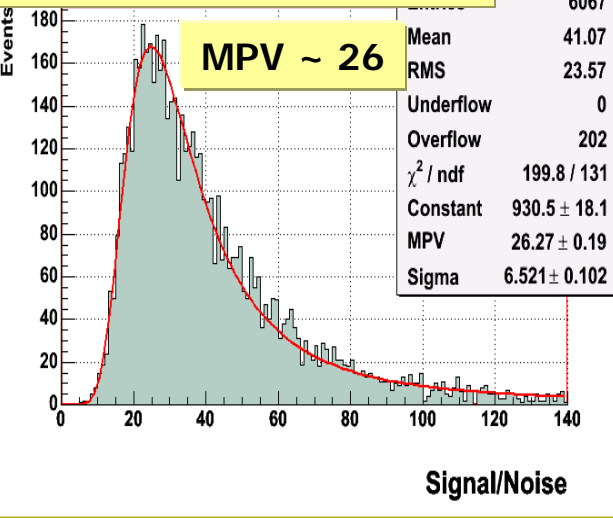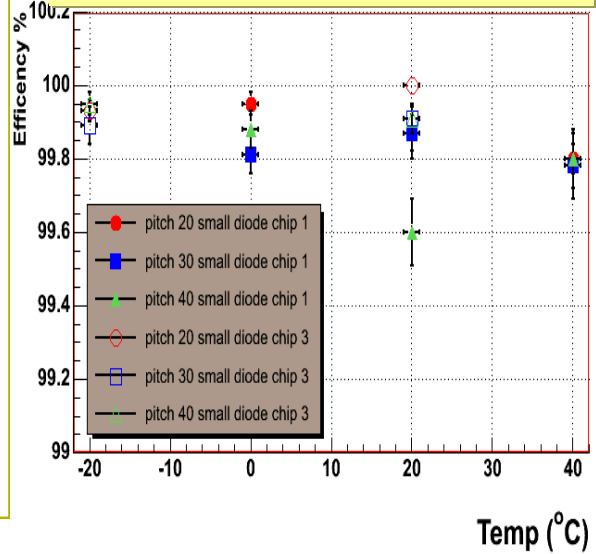| Layer	Pitch	$t_{r.o.}$	N_{lad}	N_{pix}	P_{inst}^{diss}	P_{mean}^{dis}
L0	20 μm	25 μs	20	25M	< 100 W	< 5 W

Overview of Achieved Performances

- Several MIMOSA prototypes (Strasbourg et al.) tested with H.E. beam (SPS, DESY) → well established performance:
  - N ~ 10 e-, S/N ~ 20-30 (MPV) ⇨ ε_{det} ~ 99.5 % , σ_{sp} = 1.5-2.5 μm (20 μm pitch)
  - Best performing technology: AMS-0.35μm OPTO (12 μm epi layer)
  - Technology without epitaxial layer performs well (high S/N) but gives larger clusters (poor hit separation)
  - Macroscopic sensors: MIMOSA V(1.9x1.7cm^2 ; 1Mpix), CAP-3(0.3x2.1cm^2 ; 120kpix)
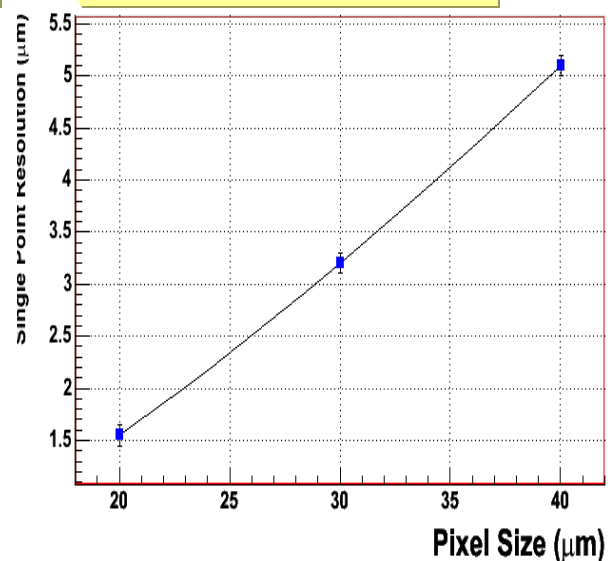
M9: S/N in seed pixel

MPV ~ 26

	sn1
Entries	6067
Mean	41.07
RMS	23.57
Underflow	0
Overflow	202
χ^2 / ndf	199.8 / 131
Constant	930.5 ± 18.1
MPV	26.27 ± 0.19
Sigma	6.521 ± 0.102

Signal/Noise

M9: Efficiency vs Temp.

pitch 20 small diode chip 1
pitch 30 small diode chip 1
pitch 40 small diode chip 1
pitch 20 small diode chip 3
pitch 30 small diode chip 3
pitch 40 small diode chip 3

Temp (^{o}C)

Sp. resol. vs pitch

Pixel Size (μm)

M.Winter-FEE06

Radiation Tolerance

- <u>Transistors</u> - In modern deep submicron tech. (eventually with special layout rules) they may be rad hard up to tens of Mrads and up to fluences of 10^{15} p/cm^2

- <u>Diodes</u> - Radiation damage affects S/N.
  - Non-ionizing radiation: bulk damage cause charge collection reduction, due to lower minority carrier lifetime (trapping)
    - → fluences ~ 10^{12} n_{eq}/cm^2 affordable, 10^{13} n_{eq}/cm^2 possible
  - Ionizing radiation:
  - noise increase, due to higher diode leakage current (surface damage)
    - → OK up to 20 Mrad with low integration time (10 μs) or

      T operation < 0° C, or modified pixel design to improve it
  - charge loss also observed, technology dependent, probably related to positive charge build-up in thick oxide (under study)

Non-Ionizing Radiation

- **Irradiation with neutron/proton with fluences up to 10^{13-14} p/cm^2**
  - Charge loss at 10^{12} n_{eq}/cm^2
  - Modest increase of leakage and noise ~ 10%

Fe55-spectrum
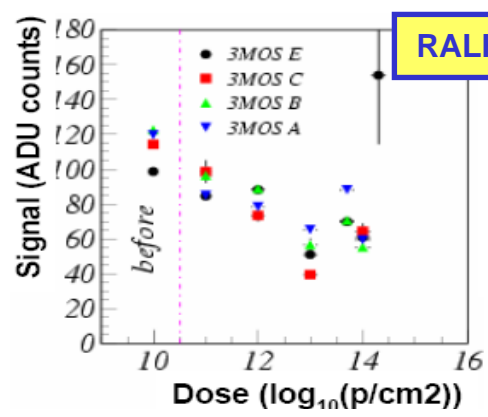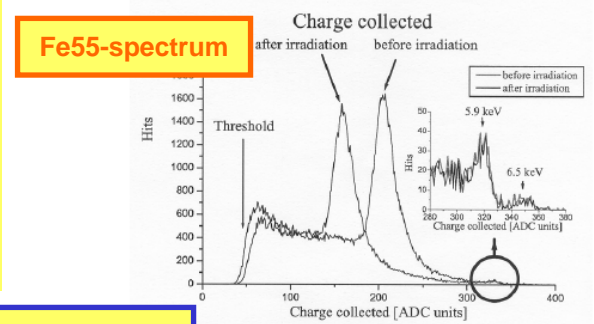
RALHEPAPS-2
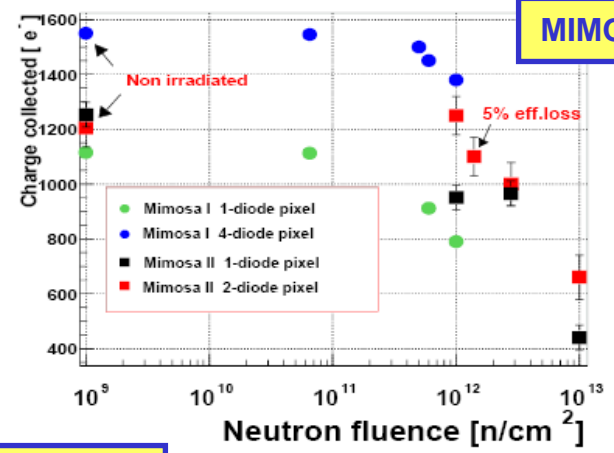
MIMOSA I-II

Charge loss correlated to the diode/pixel area ratio:
- longer distance to reach the collecting diode → higher recombination probability
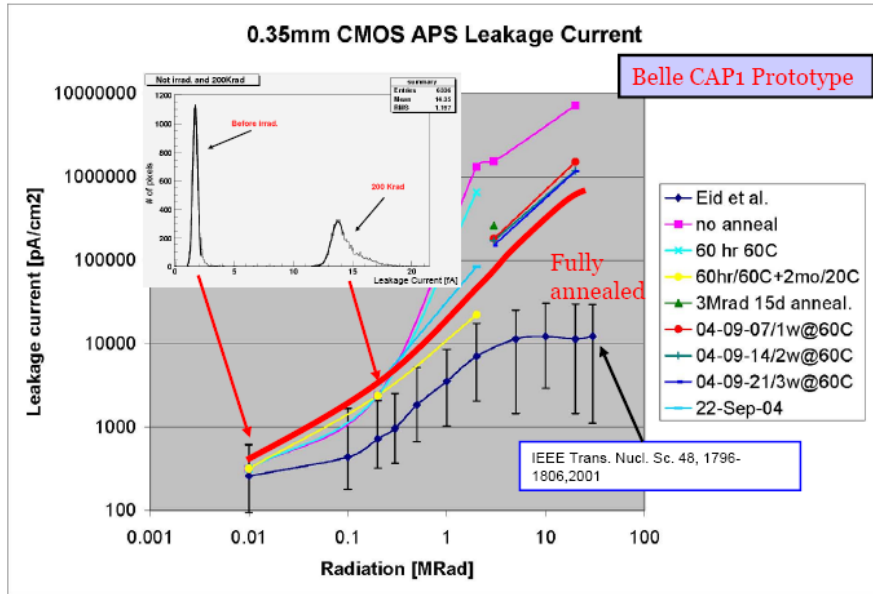- large or multiple electrodes/pixel work better

MIMOSA - AMS-0.35 OPTO (~11 um epi) test beam CERN-SPS

- S/N (MPV) vs fluence and T
- Fluence of $\geq 10^{12}$ n_{eq}/cm^2 affordable (T < 0° C) Effi det ~ 99.7 %

S/N

Fluence	T = -20°C	T = 0°C
0	28.4 ± 0.2	26.3 ± 0.2
10^{11} n_{eq}/cm^2	25.3 ± 0.2	24.5 ± 0.4
$3 \cdot 10^{11}$ n_{eq}/cm^2	—	23.0 ± 0.2
10^{12} n_{eq}/cm^2	18.7 ± 0.2	—

Ionizing Radiation Effects

0.35mm CMOS APS Leakage Current

Belle CAP1 Prototype

Fully annealed

IEEE Trans. Nucl. Sc. 48, 1796-1806, 2001

CAP (Hawaii) Prototypes irradiated with γ (^{60}Co) up to 20 Mrad

- Leakage current saturates @ 5Mrad after proper annealing.
- Noise from leakage increases:

$$V_n^2(t_{int}) = \frac{qI_{leak}}{C_D^2} t_{int}$$

- S/N reduction still modest for short integration time (<100 μs)

- Aim for short integration time and low Toperation

  OR

  modify pixel design to keep leakage current increase under control (next slide)

S/N vs dose
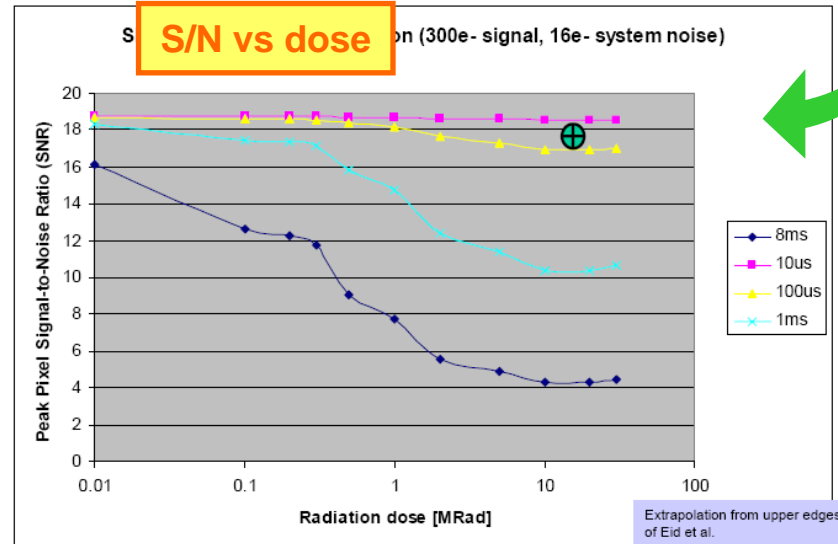
Reduce Ionizing Radiation Effects
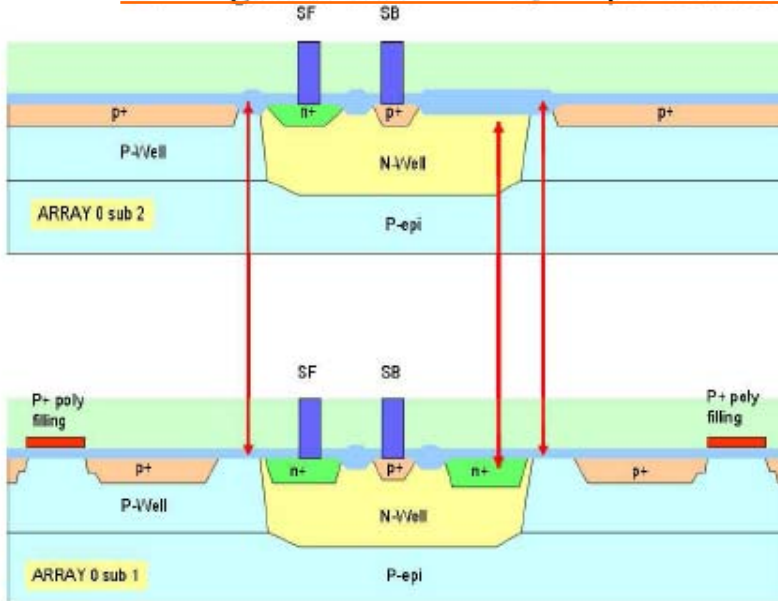
Modified pixel design

→ avoid thick oxide near the N-well

Leakage contribution for irradiated sensor is dominated by surface defects at the interface between thick oxide and silicon

10 keV X-ray

Beamtest on MIMOSA11

Running conditions: +40°C, 700μs readout time

	New	After 20kRad
Standard pixel (A0 Sub 2)		
S/N (MPV):	23.9	10.3
Det Eff [%]:	99.9	97.7
Noise [e⁻]:	10.7	23.5
Hardened pixel (A0 Sub 1)		
S/N (MPV):	14.9	15.1
Det Eff [%]:	99.5	99.6
Noise [e⁻]:	16.1	16.1

After 1 Mrad

• Noise vs. integration time and Toperation confirmed modified design is effective
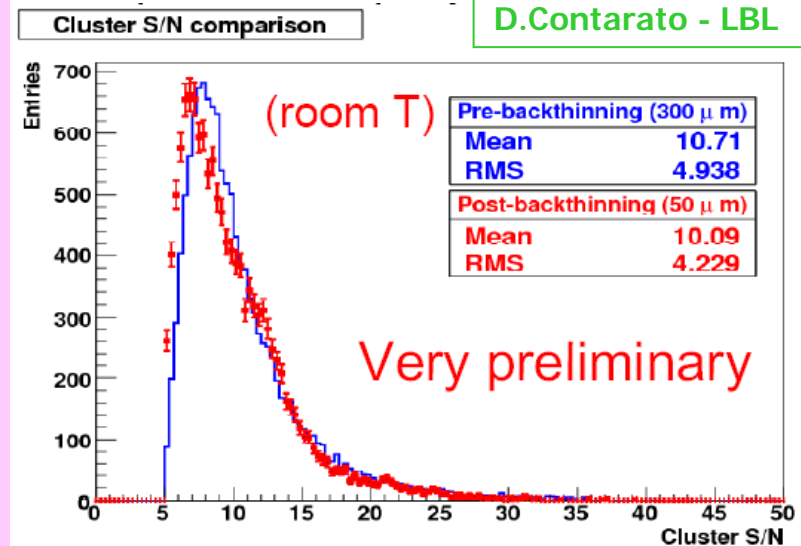
• Hardened pixel OK @ 1 Mrad at T < 0° C

Still room for improvement

Thinning

MIMOSA-5 wafers: 120 μm sensor thickness repeatedly achieved
  – ⇨ no performance loss observed (several chips tested)

➢ MIMOSA-5 chips thinned to 50 μm

  – via LBNL for STAR VD upgrade
    ⇨ Very Preliminary results
       @ room Temperature (1.5 GeV e-)

  – TRACIT company (Europe):
    • successful (mech.)
      ⇨ electrical tests foreseen

D.Contarato - LBL

Cluster S/N comparison

(room T)

Pre-backthinning (300 μm)	
Mean	10.71
RMS	4.938

| Post-backthinning (50 μm)	
Mean	10.09
RMS	4.229

Very preliminary

Entries — Cluster S/N

On going tests to thin down chips to 35-40 μm

High Readout Speed MAPS

- First MAPS prototypes realized with the basic 3T architecture and sequential readout showed very good results with M.I.P. but:
    - Extremely simple in-pixel readout configuration (3T)
    - → sequential readout → limitation for large detector: ~1 kHz sampling rate for Megapixel array

- Two main R&D directions to improve the readout speed with basic 3T readout:
    - **Pipeline design**: charge sampled and stored inside pixel at high rate (100 KHz-10 MHz) readout delayed at slower rate (only interesting time window readout, or data transferred during no beam time window) → FAPS, CAP, MIMOSA 12
    - **Parallel digital processing**: signal processing at the column level → MIMOSA 8

- Different approach: MAPS with **full signal processing at the pixel level** (**hybrid-pixel-like**), designed exploiting **triple well** option available in CMOS commercial process. Readout easily compatible with data sparsification → high readout speed potential (SLIM5 Collaboration)

Pipeline pixels

- Flexible Active Pixel Sensor (FAPS, RAL): TSMC 0.25/8, <u>10 memory cell/pixel</u>; 28 transistor/pixel; 3 sub-arrays of 40x40 pixels @20 um pitch; sampling rate up to 10 MHz; Noise ~ 40 e- rms, single-ended readout. S/N=15-17.

Cluster signal (ADC counts)
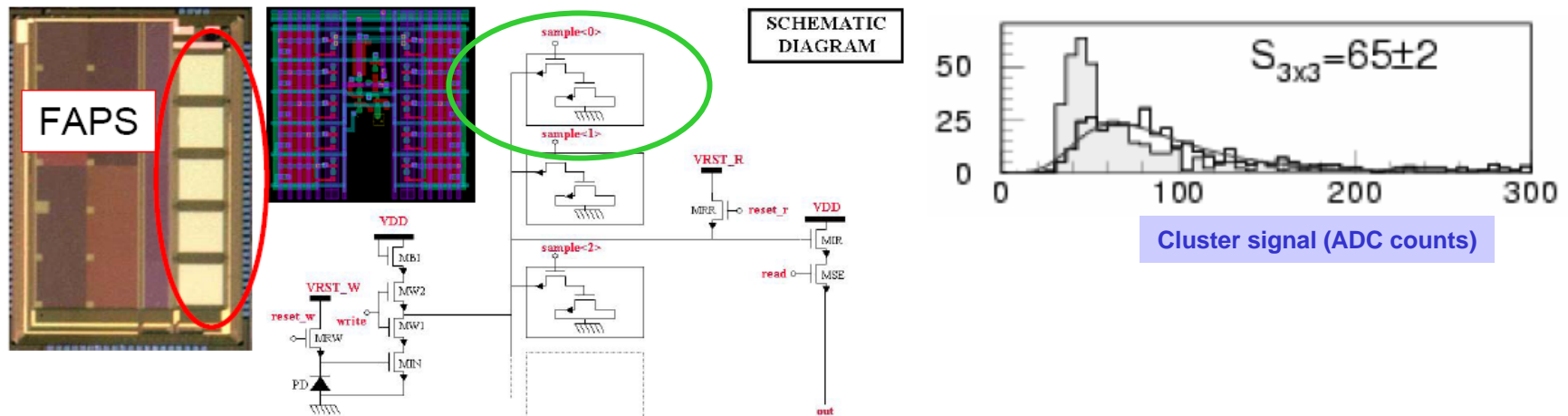
- Continuous Acquisition Pixel (CAP, Hawaii): 3 versions produced in TSMC 0.35/8 and 0.25/8, 5 pairs cell/pixel in CAP3; Noise 40-50 e- rms single ended →20-25 e- differential. Sampling rate 100 KHz with CAP2.

- MIMOSA 12 (Strasbourg et al.) in AMS 035/14: 4 pairs cell/pixel (35 um pitch) , exploring various dimensions of memory cell.

R.Turchetta-SNIC06

# Parallel read-out architecture: MIMOSA 8

- **Test beam results** (DESY, 5GeV e-)
  - Analog part
    - Typical noise ⇨ ~ 12-15 e-
    - S/N (MPV) ~ 9 ⇨ thin epi layer
    - Pixel-to-pixel dispersion ~ 8 e-
  - Digital part: the discriminator works as expected:
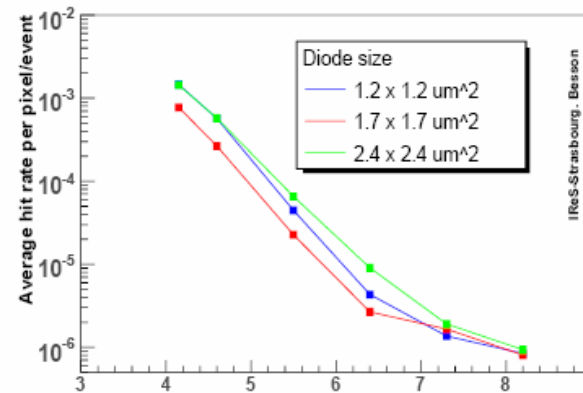
- TSMC 0.25 μm fab. process with ~ 8 μm epi layer
- Pixel pitch: 25 μm
- CDS on pixel with 2 memory cell
- 24 parallel columns (128 pixels) with 1 discriminator per column
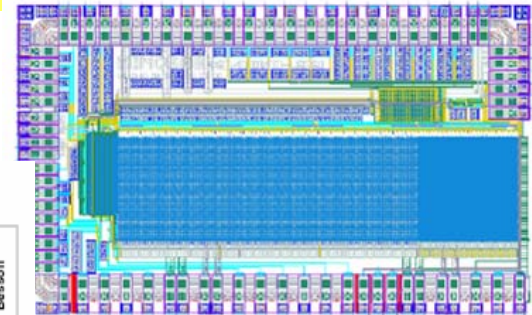- 8 analogic columns

Hit Efficiency (%) vs S/N cut
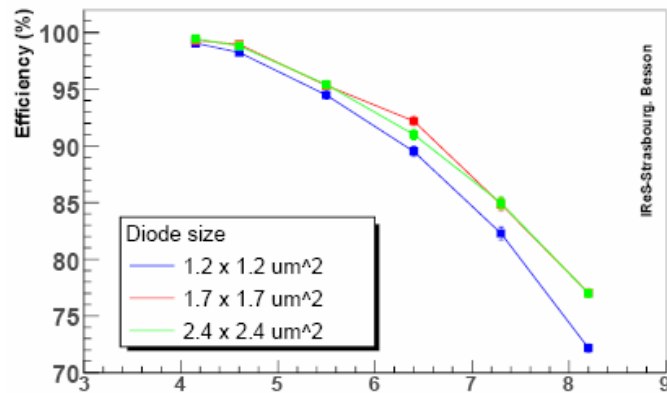
Fake hit rate (%) vs S/N cut

T = 20ºC;
r.o. clock= 40 MHz

Readout frame 20 μs
With r.o. clock= 150 MHz

⇨Excellent detection performance despite modest epi layer thickness
⇨Architecture validated for next steps: tech.with thick epi layer, rad. Tolerant pixel at Troom, ADC, sparsification etc.

Triple well CMOS MAPS (I)

- Use of commercial triple-well CMOS process proposed to address some limitations of conventional MAPS
    - improve readout speed with in-pixel signal processing
    - improve single pixel signal with a larger collecting electrode

In triple-well processes a deep n-well is used to provide N-channel MOSFETs with better insulation from digital signals
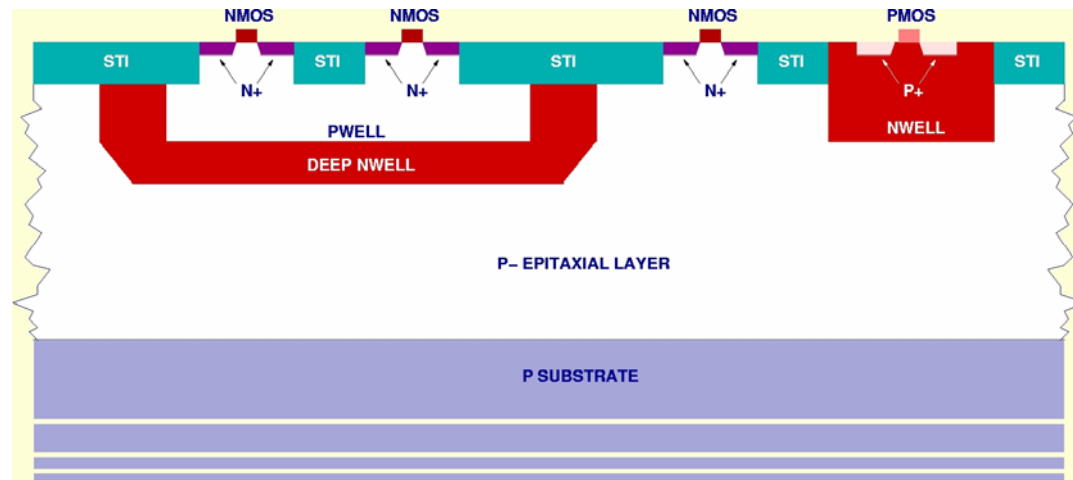

This feature exploited for a new approach in the design of CMOS pixels:

- The deep n-well can be used as the collecting electrode

- A full signal processing circuit can be implemented at the pixel level overlaying NMOS transistors on the collecting electrode area
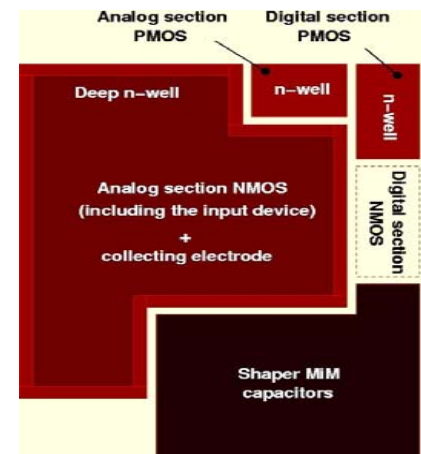
Triple well CMOS MAPS (II)

♦ **Standard processing chain for capacitive detector implemented at pixel level**

- Charge preamplifier used for Q-V conversion:
  - Gain is independent of the sensor capacitance -> collecting electrode can be extended to increase the signal
- RC-CR shaper with programmable peaking time (0.5, 1 and 2 μs)
- A threshold discriminator is used to drive a NOR latch featuring an external reset
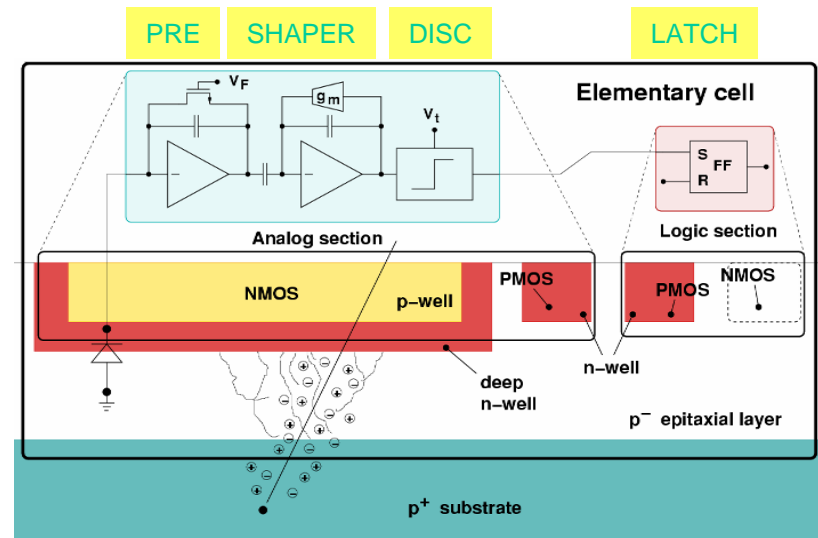
- Fill factor = deep n-well/total n-well area $\geq$ 0.85 in the prototype test structures $\rightarrow$ high detection efficiency

♦ **Readout scheme compatible with existent architectures for data sparsification at the pixel level -> improve readout speed**
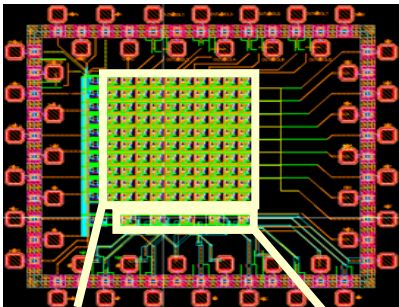
Triple Well MAPS Results

Noise only (no source)

- **First prototype** chip, with **single pixels**, realized in 0.13 μm triple well CMOS process (STMicrolectronics)

- Very encouraging results:
  - Proof of principle
  - S/N = 10 (^{90}Sr β source)
    - Single pixel signal ~1250e- (only 300 e- in conventional MAPS!)
    - High pixel noise ENC = 125 e- (due to underestimated deep nwell capacitance)

threshold

Landau peak 80 mV

saturation due to low energy particle.

1250   2200   3000 (e-)
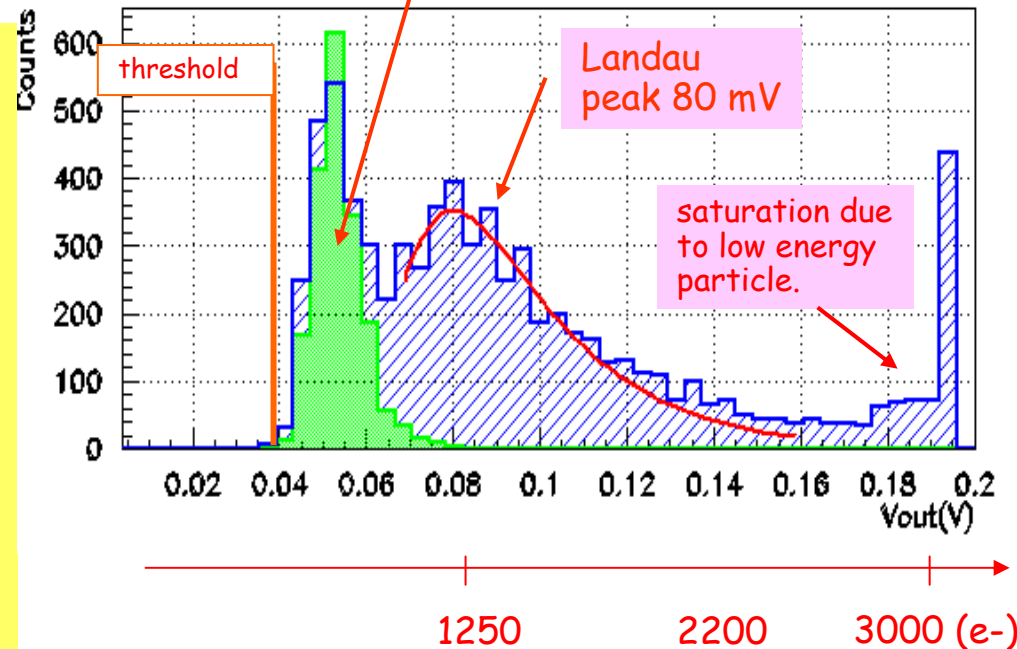
Second prototype under test:

- Pixel matrix (8x8, 50x50 μm^2) with simple sequential readout tested up to 30 MHz.
- Pixels with varying electrode size (900-2000 μm^2)
- Improved front-end: pixel noise ENC = 50 e-
  → M.I.P. Expected S/N ~ 25
- Problems: threshold dispersion measured ~300 e-, ground line bouncing in digital transitions.

8 x 8 matrix + dummies

Single pixel test structures

Next steps for triple well MAPS

- Final ambitious goal of the SLIM5 Collaboration is to design a monolithic pixel sensor with similar readout functionalities as in hybrid pixels (sparsification, time stamping), suitable to be used in a trigger (L1) system based on associative memories. →Test beam in 2008.

- First triple well MAPS prototypes (0.13 μm-ST), with full signal processing at the pixel level, demonstrated capability to detect ionizing radiation with good S/N.

- Next prototypes (Aug-Nov '06) will improve significantly threshold dispersion (to noise level) and test readout architecture with data sparsification and time stamp.

- Radiation Tolerance should still be investigated:
  - Design with large collecting electrode expected to be more rad hard against non-ionizing radiation.
  - Charge preamp. with continuous reset less sensitive to leakage current increase from ionizing radiation

Applications of MAPS in future experiments

- First detectors made of CMOS MAPS coming soon:
  - MIMOSA sensors will equip
    - STAR Heavy Flavour Tagger:
      - 2008 analog output, 4 ms readout time
      - 2011 digital output ~ 200 μs frame r.o. time
    - EUDET beam telescope for ILC R&D:
      - 2007 demonstrator with analog output
      - 2008 final device with digital output

- CMOS MAPS developed also for:
  - ILC Vertex Detector: R&D France, UK, USA, Italy…
  - SuperBFactory Vertex Detector: R&D in Hawaii (Belle), Italy (BaBar)

Conclusions

- Future vertex detectors need a new technology (granular, thin, fast…) and CMOS sensors could potentially accommodate all the requests
- Excellent tracking performance established in the first years of R&D on CMOS MAPS
- The MAPS community, very active and still growing, has still a lot to do in the coming years to convert a good idea into a real operating detector for the most challenging applications
- Main R&D directions:
  - High readout speed MAPS, digital output & sparsification
  - Radiation tolerance
  - Thinning procedure
  - New fabrication processes