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Wafer-level CMOS post-processing

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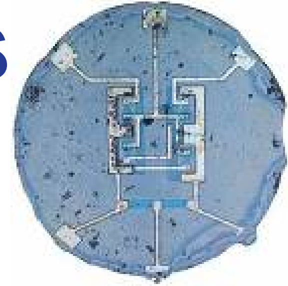
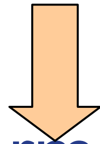
Outline

- Introduction on wafer-level post-proc.
- CMOS: a smart, but fragile substrate
- Post-processing steps
- System examples
- Conclusions

45 years of integrated circuits



Enormous skill in micro-manufacturing



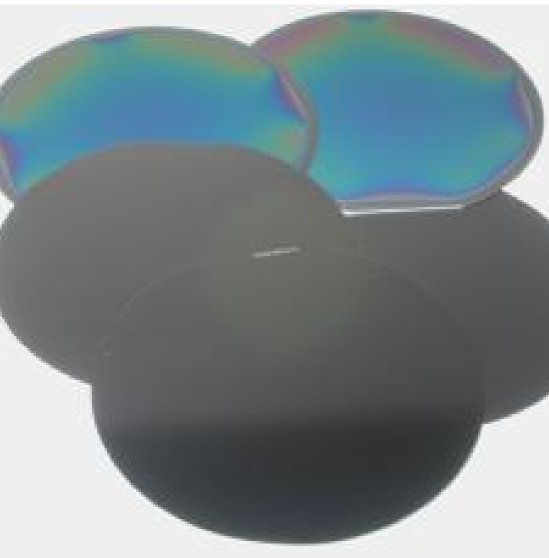
- High performance computing
- Solid-state memories

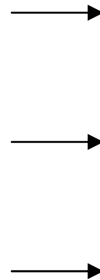
Can we do more with this skill than number crunching and memorizing?

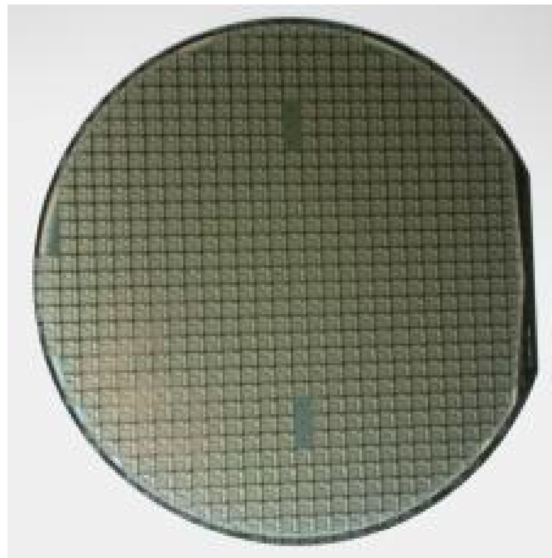
One approach: wafer level post-processing

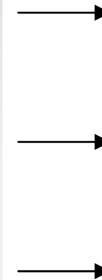
Wafer-level post-processing

Add process steps only here









"There's plenty of room at the top"

The idea of CMOS post-proc. (1)

Wafer-scale post-processing:

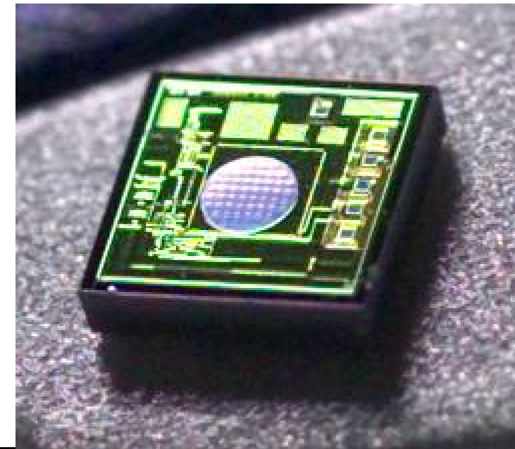
- Chips are finished and fully functional
- No intrusion into “clean” IC fab
- Still benefit from planar technology (yield, efficiency, cost, existing toolkit…)
- A microchip is fragile, so take care!

The idea of CMOS post-proc. (2)

Attractive when:

- The monolithic solution is cheaper (saving assembly & testing expenses)
- The monolithic solution outperforms hybrid technologies
- Size matters

See www.akustica.com



Is post-processing trivial?

1. The chip is vulnerable:
   - Heat > 400 ºC destroys the metallization
   - Plasma charging destroys the MOSFETs
   - Mechanical stress changes components
   - H_2 passivation must be maintained
2. Packaging has to be re-invented.
   Without package: contamination…
3. How to deposit high-quality thin films?

High temperature in IC fabrication

Heat is necessary during IC fabrication:

- To oxidise silicon
- To diffuse impurities in silicon
- To repair silicon lattice damage
- To activate impurities
- To deposit materials by CVD
- To initiate reactions, e.g. $Ti + 2Si \rightarrow TiSi_2$

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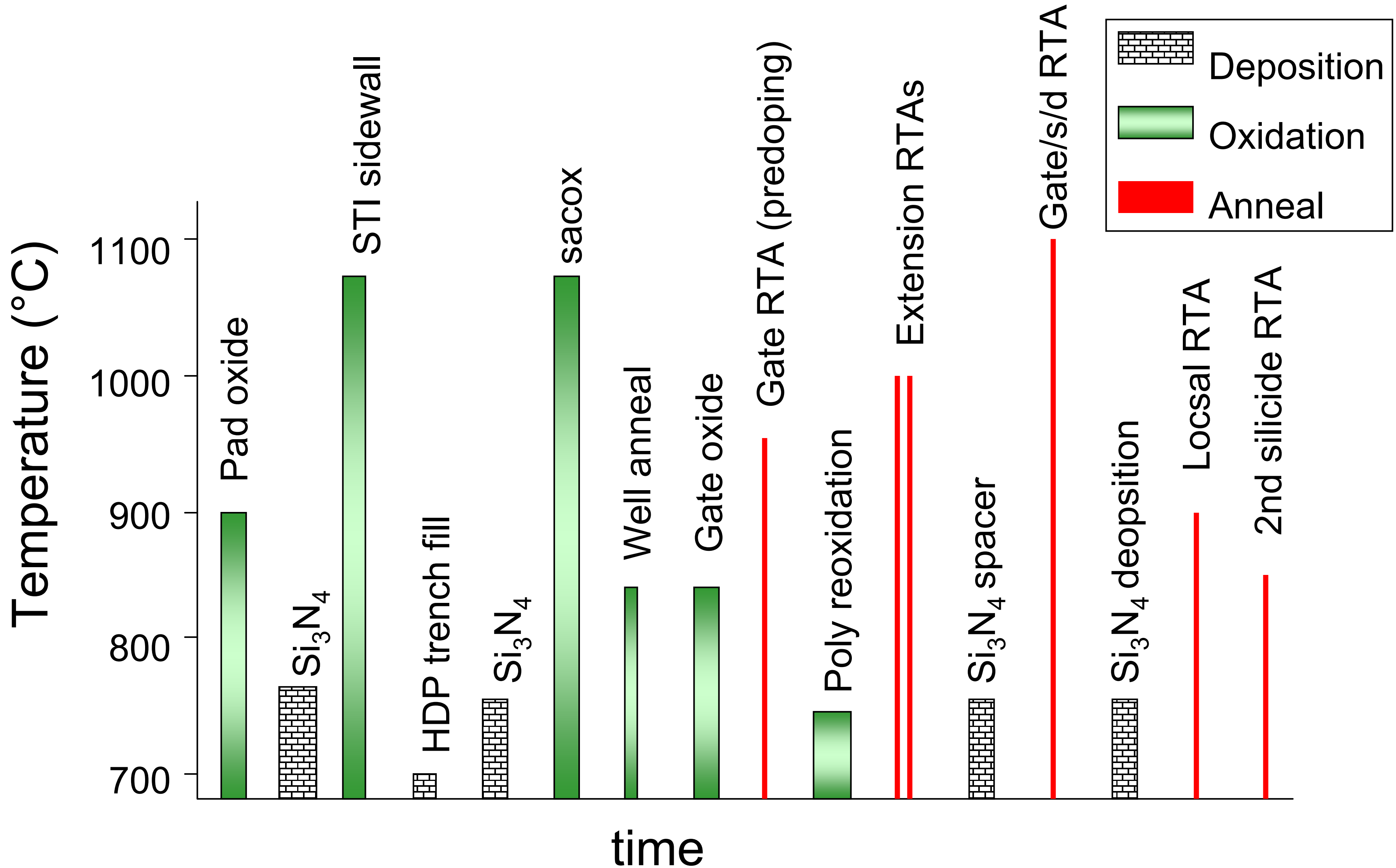
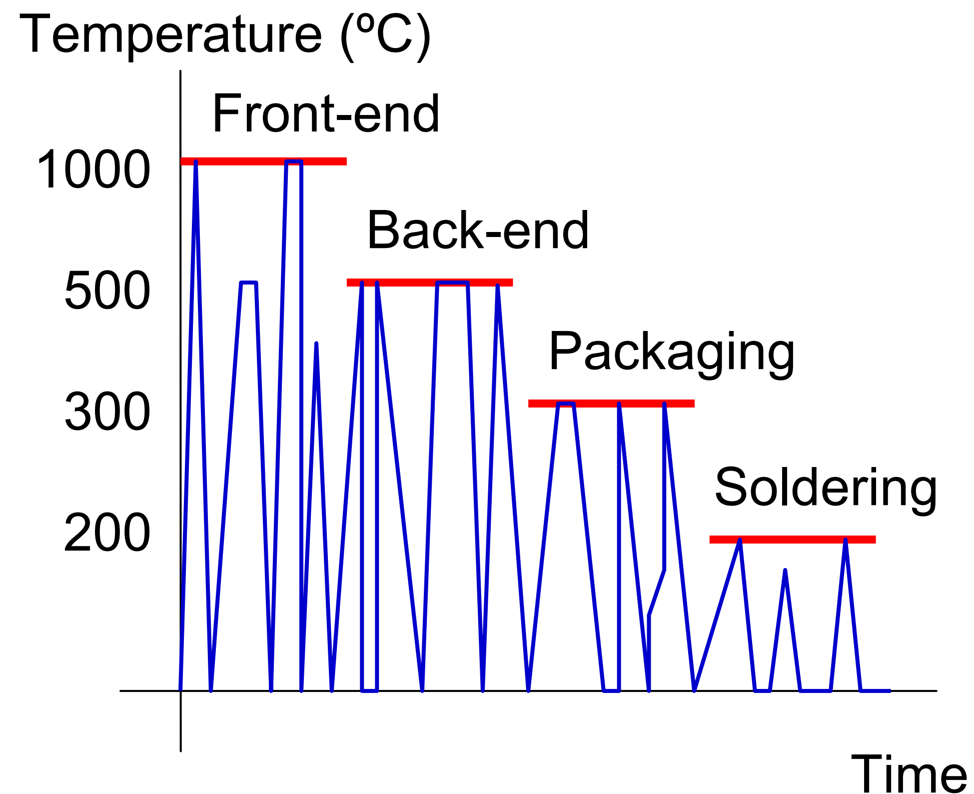


Thermal budget of an IC

Keep it cool(er)

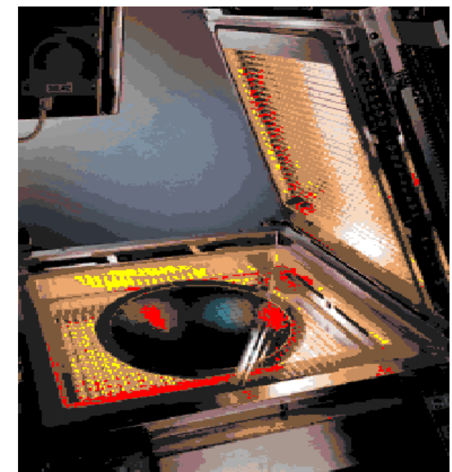
- Transistor ready: stop diffusion
- wires ready: avoid Al melt
- Soldering ready: avoid solder melt



Thermal budget trend

- Smaller dimension transistors: diffusion should be reduced
- High-temperature steps are reduced in time and temperature, where possible

New machines (RTP, laser)
New materials (SiLK)
New techniques (ICP-CVD)



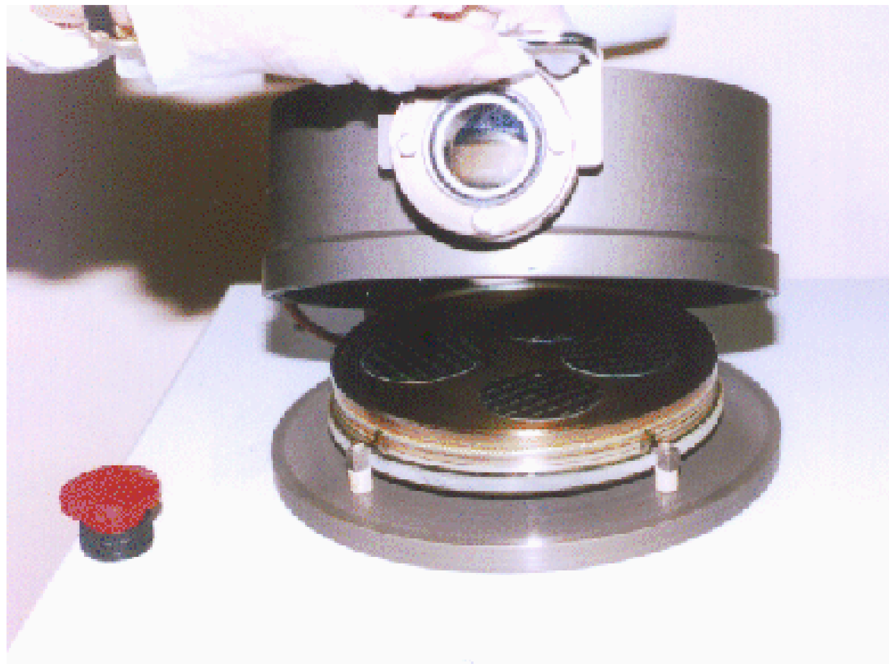
(Post) process-induced damage

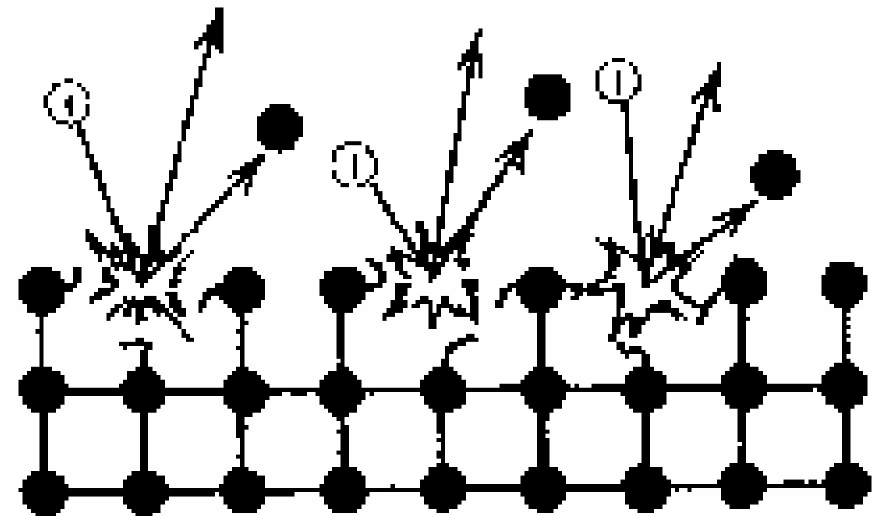
- Mechanical damage (e.g. scratches)
- Electrostatic discharges
- Plasma damage in IC technology:
  - Plasma etching
  - Plasma-assisted depositions (PECVD)
  - Photoresist removal

All three: hard to do without!

Plasma etching

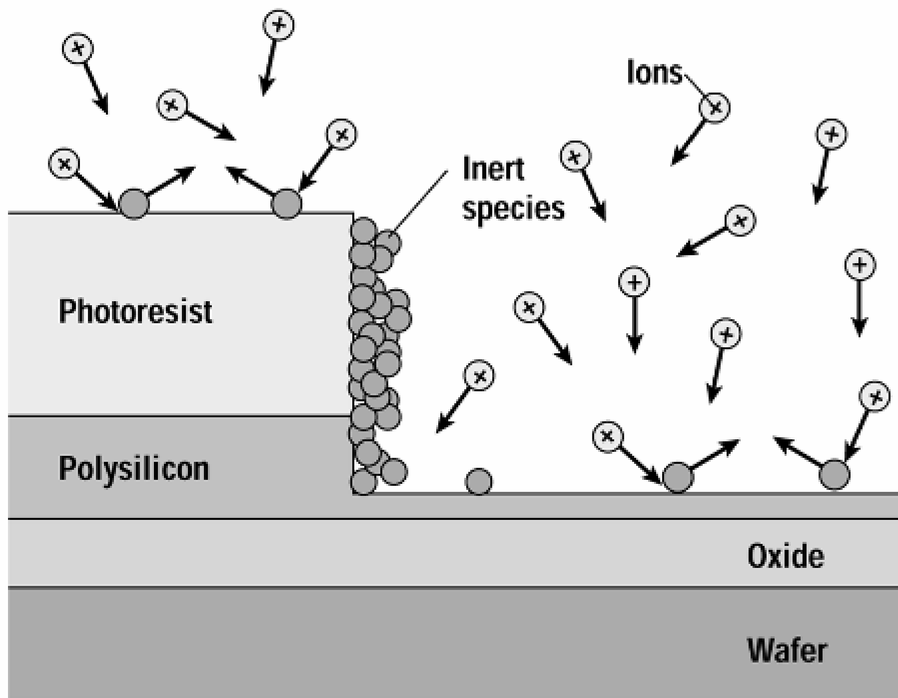
- Ions bombarding the surface
- Radicals reacting with atoms



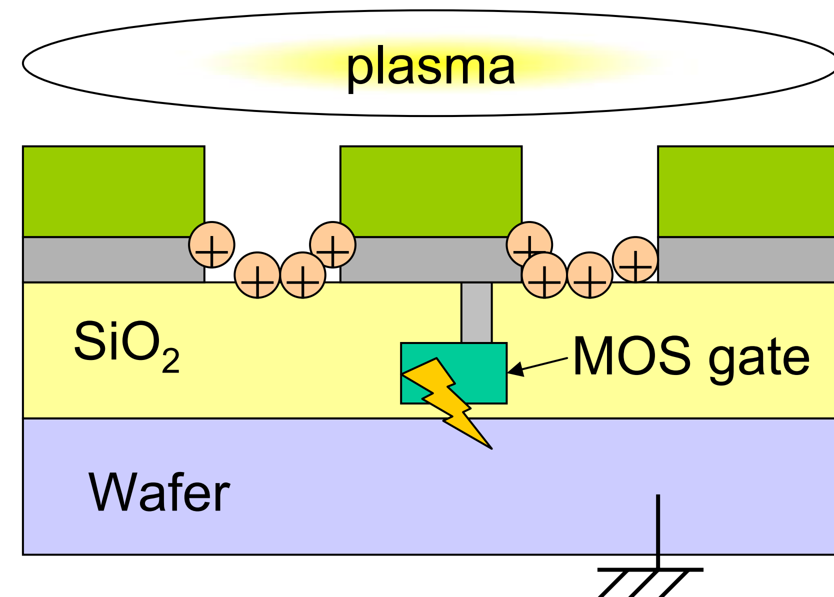


Plasma etching induced damage

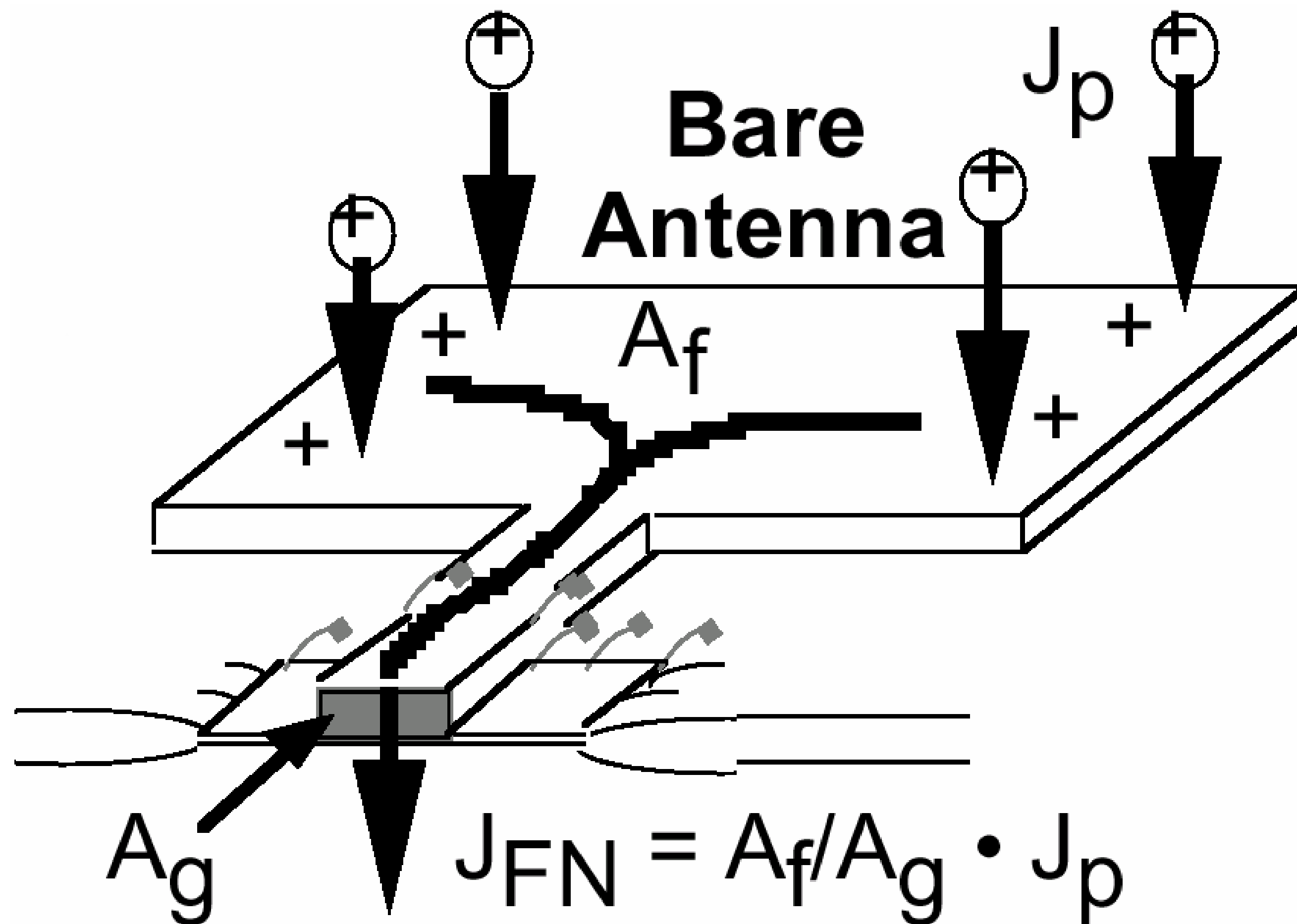
- High anisotropy → vertical profiles



Charge pile-up can lead to discharging inside the chip



The antenna effect



Plasma processing induced damage

Suppression:

- Adopt design rules
  (unfit for wafer-scale post-processing)
- Tune the plasma settings
- Use other approach
  (e.g. remove photoresist in a liquid)

Other alerts

- H_2 passivation essential for MOSFET
  - Final alloy step (30’ 400 ºC in H_2/N_2)
  - Hot processing leads to H_2 outgassing
- Mechanical stress should stay low
- Metal ions can ruin the chip, even at room temperature!
  →Stick to IC mfg. rules

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May we introduce a new material?

[1980s]

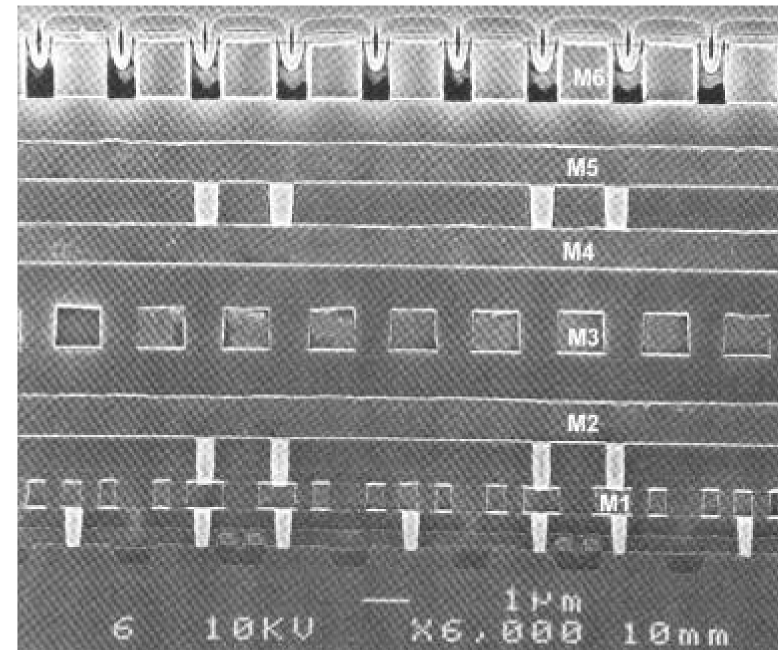
[1990s]

[2000s]

(source: www.intel.com)

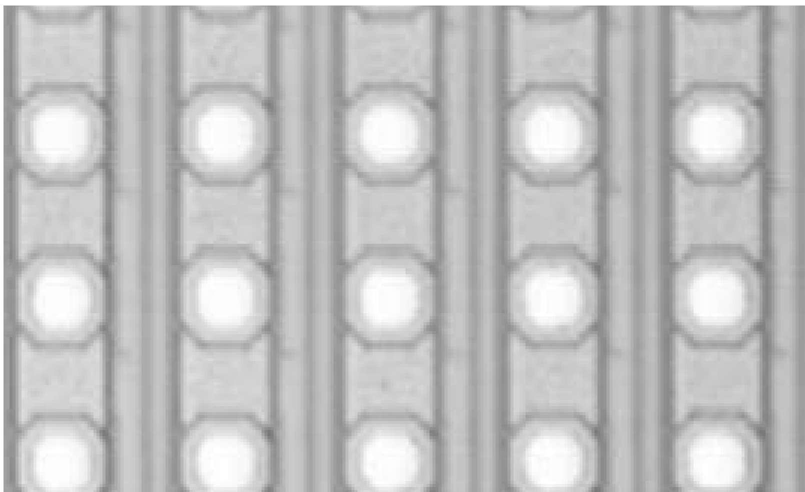
What is allowed above CMOS?

- All backend tricks can be repeated!
  - Metal deposition
  - Dielectric deposition
  - CMP
  - Patterning
- Semiconductors?
- Polymers?
- Suspended structures?

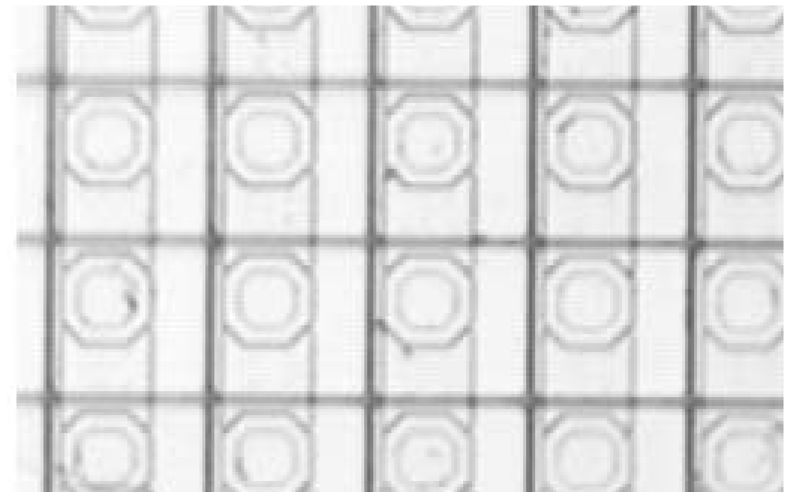


Example: Medipix2 modification

- Technique: wafer-level lift-off lithography, using aluminum
- Result: Medipix2 still fully functional



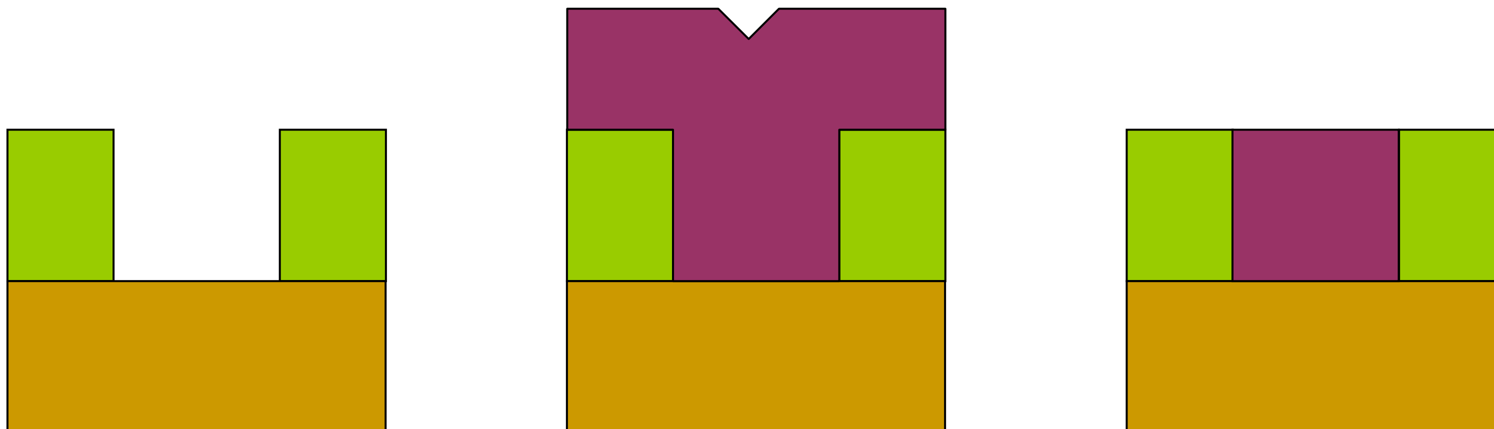
Good for ball-grid-arrays



Good for gaseous particle detection

CMOS post-proc. steps (3)

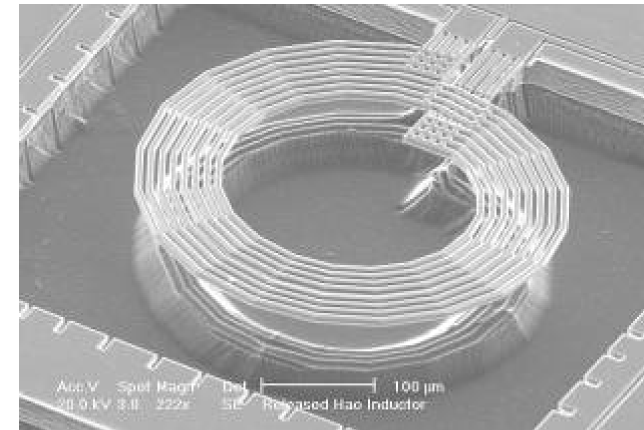
- Chemical Mechanical Polishing allows to pattern “any” new material
- E.g. piezo-electric films, ferro-electrics



Dielectric and semiconductor thin films

- Some activation energy is necessary to form strong bonds
- Low-temp depositions: ECR-CVD, ICP-CVD
- Laser crystallization?

Suspended structures



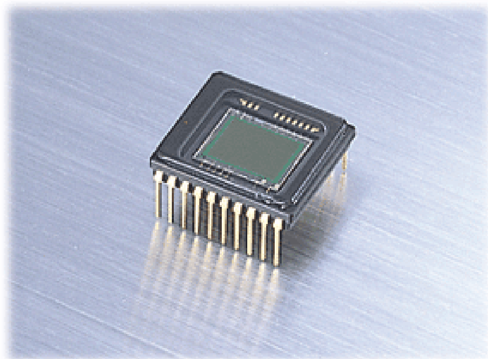
- Sacrificial material:
  - SU8
  - SiGe (T. J. King et al., UCB)
  - BCB
  - Parylene
- Structural material:
  - rigidity
  - residual stress → impact on IC

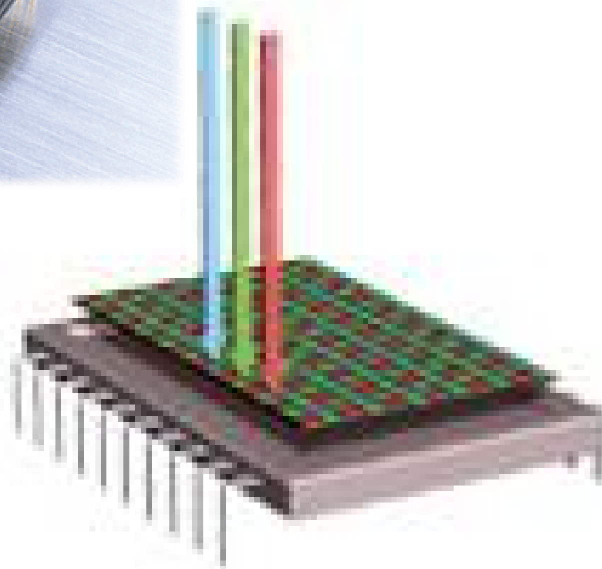
wlpp microsystems

- CMOS image sensor
- LCOS
- Micromirrors
- Ultrasound imaging detectors
- SIAM X-ray detectors
- Integrated Micromegas
- Integrated microchannel plate

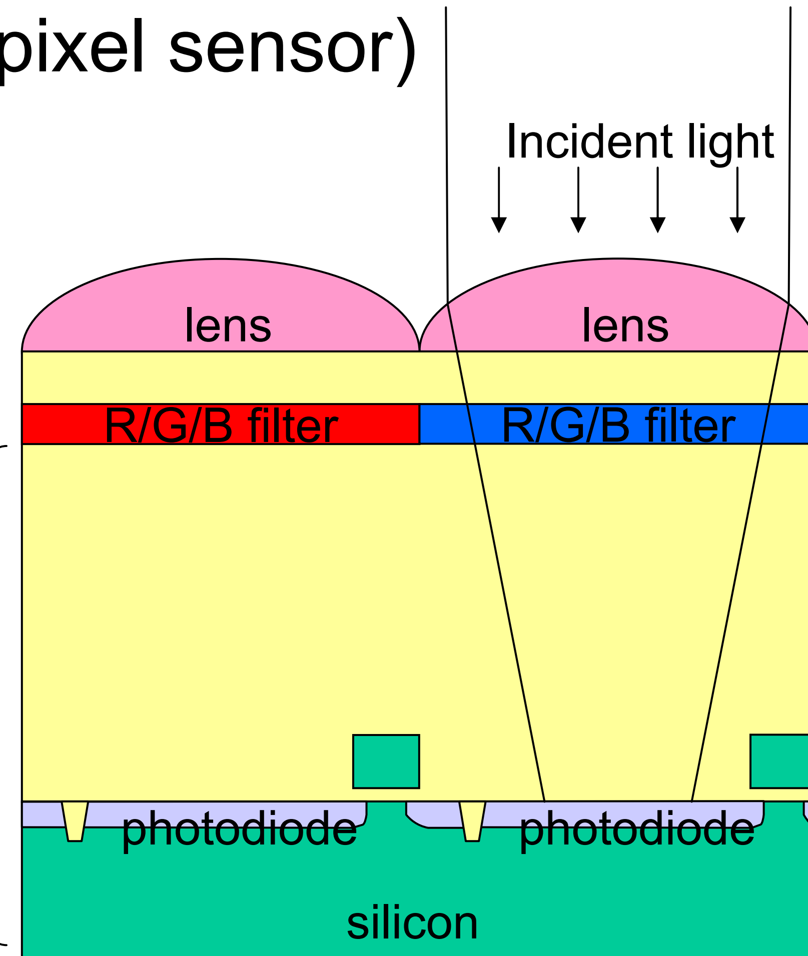
The CMOS image sensor

(= monolithic active pixel sensor)



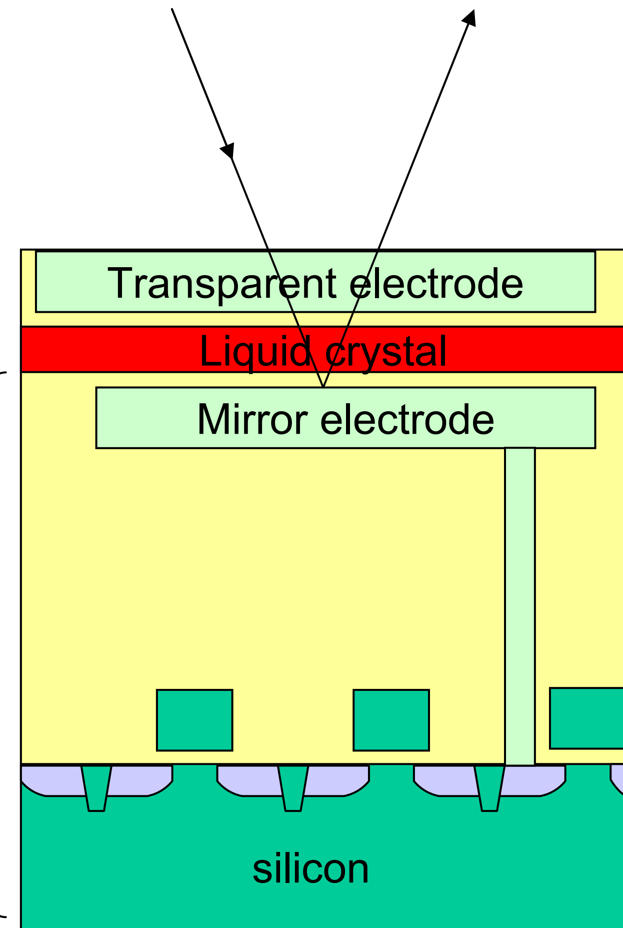


Standard CMOS

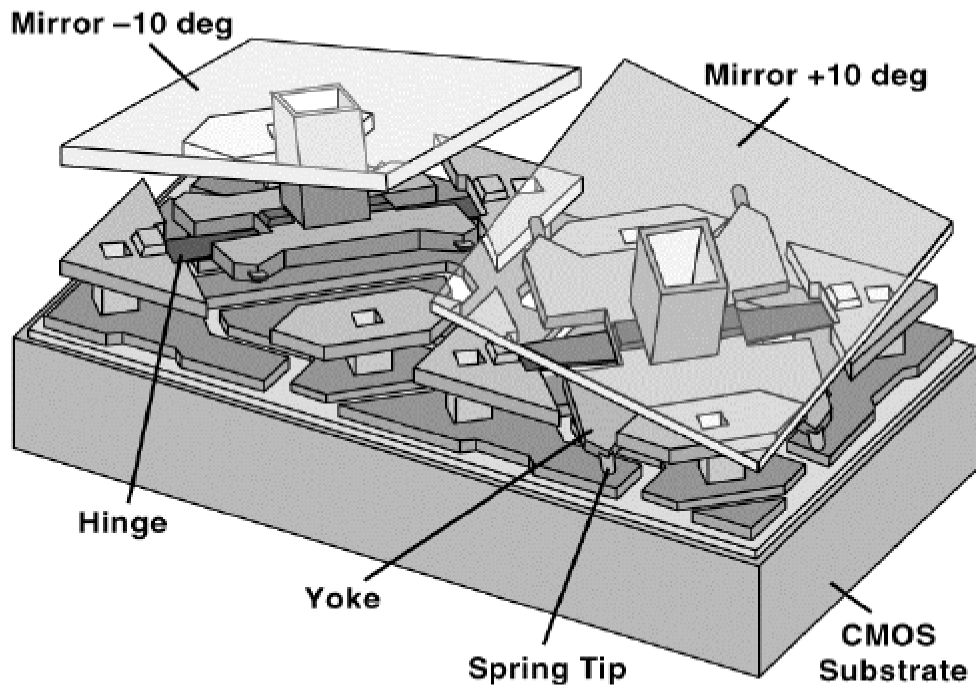


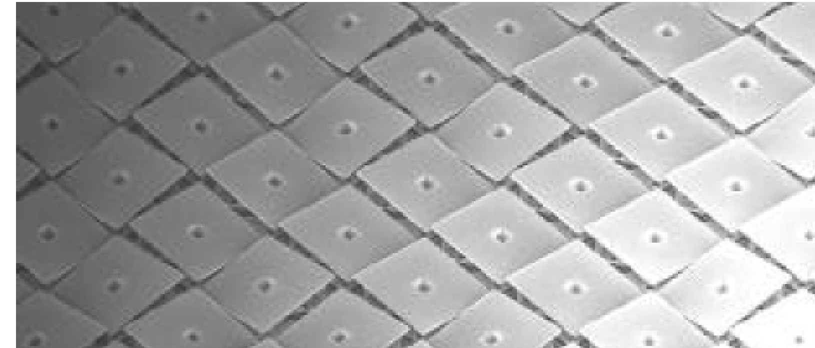
Liquid crystal on silicon (LCOS)

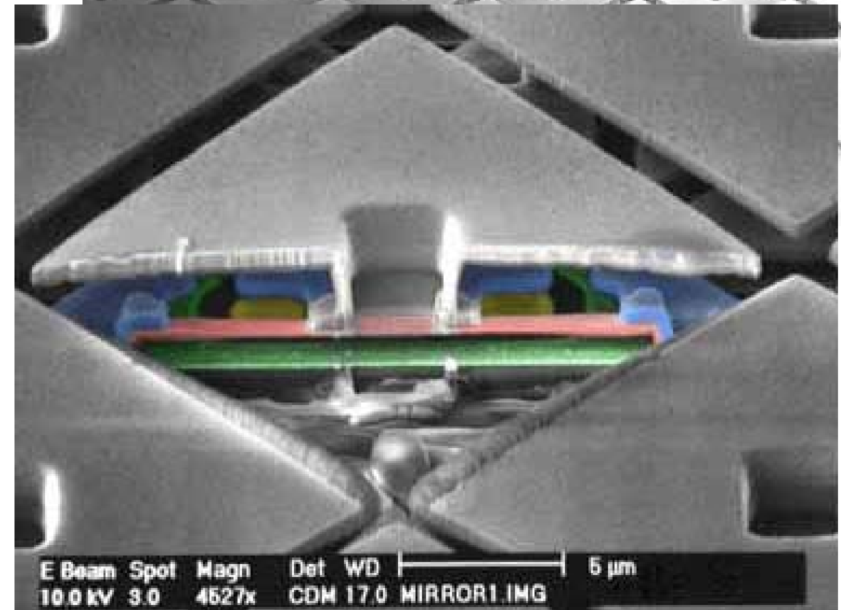
Standard CMOS



TI’s micromirrors







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CMOS DMOS-4

CMP

Metal3

SPCR1

VIA

Hinge & Yoke (Beam)

SPCR2

VIA

Mirror

Wafer Partial SAW

Plasma Undercut

Passivation

To Test

Wafer Break

Done

Die Attach and Bond

Plasma Activation

Passivation

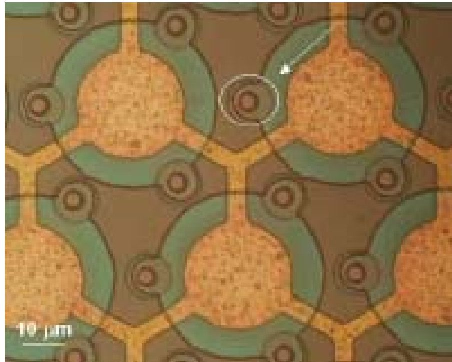
Window

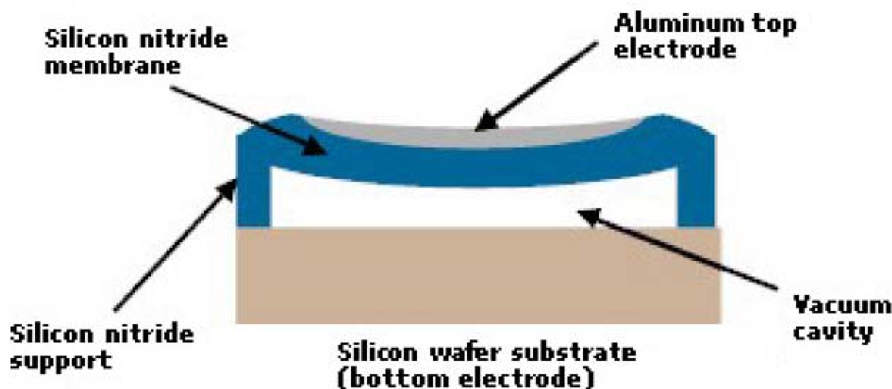
T2/Burn-in

T3/Test

Ultrasound detector arrays

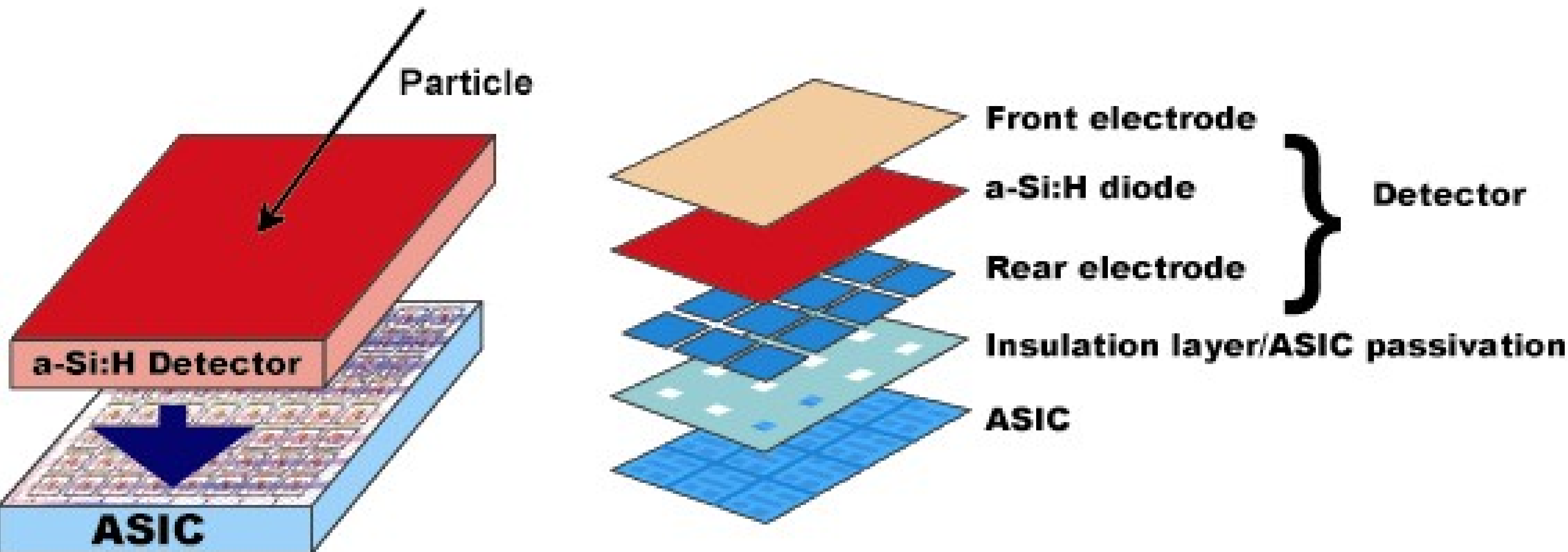
Sensant (now acquired by Siemens)





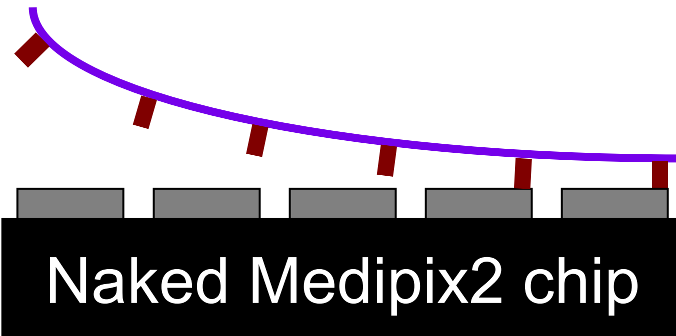
Monolithic X-ray detector

- SIAM collaboration

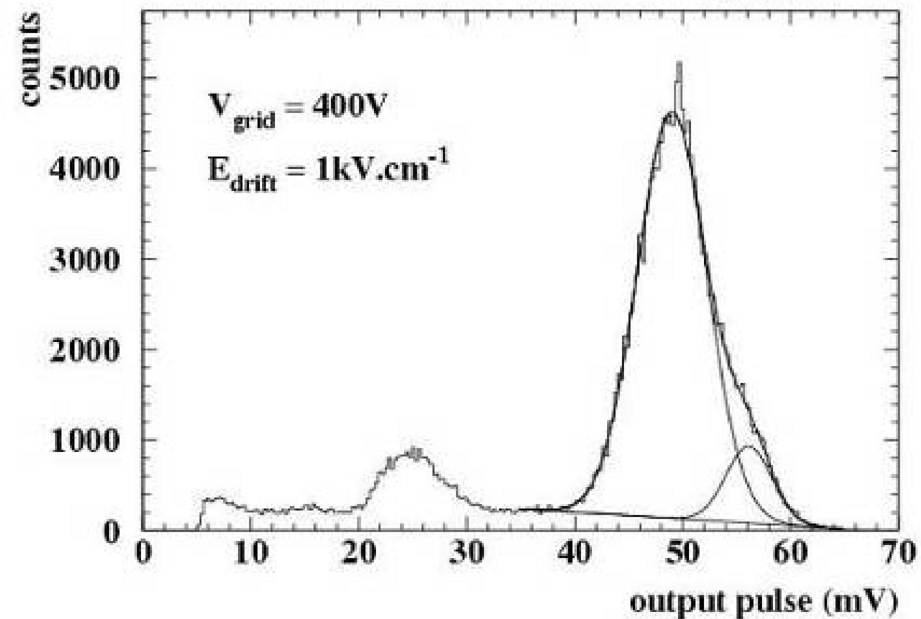


http://asi-hdet-project.web.cern.ch/asi-hdet-project/

The GOSSIP gaseous detector

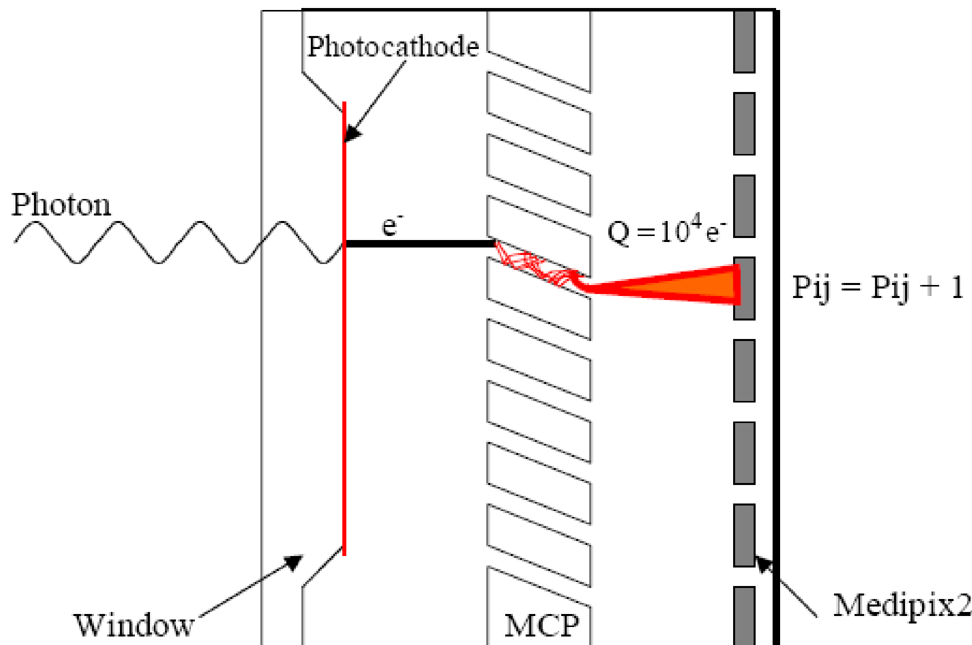


V. Carballo Blanco et al., IWORID 2006

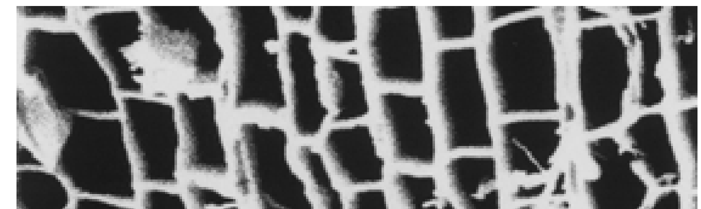


Integrated microchannel plates

Principle: J. Vallerga et al., IWORID 2004



Wafer-level manufacturing:
Porous alumina?



Naked Medipix2 chip

J. Melai et al., IWORID 2006

Conclusions

- IC Technology now offers a wide range of manufacturing techniques
- Computing and data storage **+ extra's**
- Many new microsystems under study
- Our focus: systems with high internal data rates → wiring is not an option

Acknowledgements

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